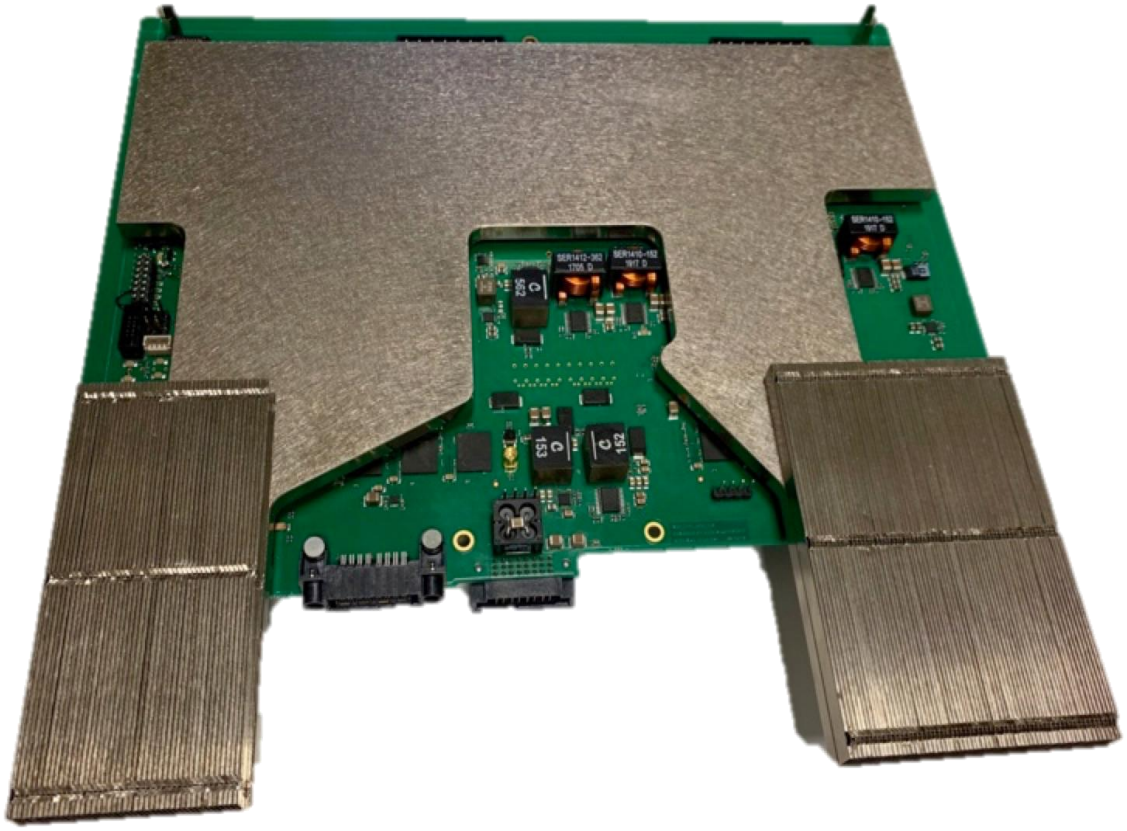
SKA iTPM-ADU V1.6 Board
User Manual



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Sandro
Pastore

DOCUMENT CHANGE RECORD

Issue	Date	Paragraphs affected	Change information
1.0	1/09/2019	All	New document
1.1	20/02/2020	All	Updated to board revision 1.6

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1. SCOPE

Purpose of this document is to introduce the designer to the usage of the iTPM (Italian Tile Processor Module) ADU (Analog to Digital Unit) Board revision 1.6 of SKA (Square Kilometer Array). It provides information about the board components, the main functions and interfaces, the mechanical, electrical, power characteristics and the board start-up.

The document is organized as follows: an overview, the board mechanical and electrical characteristics, the main features, interfaces and interconnections among main building blocks (the complete pinout [RD2] and connection table of the larger devices – chapters 8 and 9 - are available), information about power consumption, configuration details of the main programmable devices, and description of the board power up sequence.

2. ACRONYMS

AD	Analog to Digital
ADC	Analog to Digital Converter
ADU	Analog to Digital Unit
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
COTS	Commercial Off The Shelf
DDR	Double Data Rate
EEPROM	Electrically Erasable PROM
FSPI	FPGA SPI
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
HW	Hardware
IF or I/F	Interface
IO or I/O	Input/Output
IP	Intellectual Property
ITPM	Italian Tile Processor Module
MAC	Media Access Control
Mbps	Mega bits per second
MIPS	Million of Instruction Per Second
PLL	Phase Locked Loop
PPS	Pulse per second
QSFP	Quad Small Form-factor Pluggable
RAM	Random Access Memory
SDRAM	Synchronous DRAM
SMA	SMA (SubMiniature version A)
SPI	Serial Peripheral Interface
SRAM	Static RAM
STD	Standard
SW	Software
SKA	Square Kilometer Array
TBC	To Be Confirmed
TBD	To Be Defined
UDP	User Datagram Protocol

3. APPLICABLE AND REFERENCE DOCUMENTS

3.1 APPLICABLE DOCUMENTS

[AD1] SKA-TEL-LFAA-0500001 SP-COR-DD Rev 01 Signal processing design document.pdf

3.2 REFERENCE DOCUMENTS

[RD1] SKA_R1.1_mec_pcb.pdf – mechanical PCB drawing, not currently available
[RD2] Digital devices configuration and I/O connections: TPM_ADU_1_6_PINOUT.xlxs
[RD3] SKA_Subrack_Specification document.docx
[RD4] AAVID boyde, cooling solution for SKA Subrack, BVE74 - Rev 12.pdf
[RD5] AAVID boyde, ADU1.5 heat sink custom design, AAVID_BG569 - Rev 6.PDF
[RD6] Samtec Fly-OVER cable product-sheets:
www.samtec.com/cables/high-speed/assemblies/qsfp-flyover
[RD7] iTPM_ADU_1_6_TOPO_TOP.pdf
[RD8] iTPM_ADU_1_6_TOPO_BOT.pdf
[RD9] FQSFP ADU1.5 EXPANSION.pdf
[RD10] LFAA Backplane schematic: ska_backpl_v01_1.pdf
[RD11] iTPM1.6 Register Map : iTPM16_RegisterMap_BiosVersion0.0.5.docx

4. OVERVIEW

The iTPM (Italian Tile Processor Module) is the Tile Processor Board of the Square Kilometer Array. It is a 32-channel 1GHz 8/12 bit Analog to Digital conversion/preprocessing board, equipped with management functions to support the integration into the rack structure.
Best-in-class 14 bit AD converters, last 16nm FPGA, 40Gbit Ethernet optical link have been selected focusing on the best commercial compromise between quality, performance and power consumption.
Compact board size, low noise clock network, advanced 14-layer board build-up, complete Ethernet based management features (including health monitoring capability), high efficiency and low noise power distribution system complete the main board features.
The iTPM provides also external synchronization signals and high speed DDR4 memory banks to allow RAW data buffering.
An on-board 32 bit microprocessor and large flash memories allow high-level management operations including on line multiple configuration selection and structured communication with infrastructure management applications.

The iTPM board is provided with a low-level management firmware to perform board configuration and monitoring through the Ethernet interface exploiting a UDP based protocol.

The following list sums up the remarkable iTPM characteristics and features:

- Compact size, 6U format, designed for backplane installation
- Thirty-two analog inputs capability with high quality and high isolation stackable RF 50Ohm input connectors
- Thirty-two optional analog programmable drivers (amplifier/attenuator, not present on default configuration)
- Sixteen dual channel 14 bit 1Ghz AD converters
- High quality clock distribution system with full JESD204B Subclass 1 capability on all inputs, with deterministic latency between the channels and the user configurable low noise PLL
- Two Xilinx Ultrascale XCKU9P 16 nm FPGA devices dedicated to data processing, implementing the same functionality, managing 16 channels each
- Two DDR4, 64 bit memory banks, up to 16+16 GByte total size
- Two 40G Ethernet interfaces (QSFP), one for each FPGA
- High speed internal bus to connect the 2 FPGAs, up to 75 Gbit + 75 Gbit bidirectional
- Low-level Ethernet gigabit management interface with instant ON flash based Lattice CPLD
- Complete system monitor interface with power, voltage and temperature monitoring
- On board two 256Mbit SPI user flashes for multiple FPGA configuration options
- Second level management microprocessor (ARM Cortex M0+, 32 bit, 48 MHz) for high-level remote board control
- High efficiency multistage Power Distribution system, with configurable start up and power sequence. Compatible with Xilinx JTAG Virtual cable capability for complete remote debugging based on the Ethernet gigabit management link

5. MECHANICAL OVERVIEW AND BOARD LAYOUT

5.1 Mechanical Overview

iTPM-ADU 1.6 fits a 6U high and 179 mm depth standard rack mount format compatible with the SKA LFAA Subrack mechanical specification.

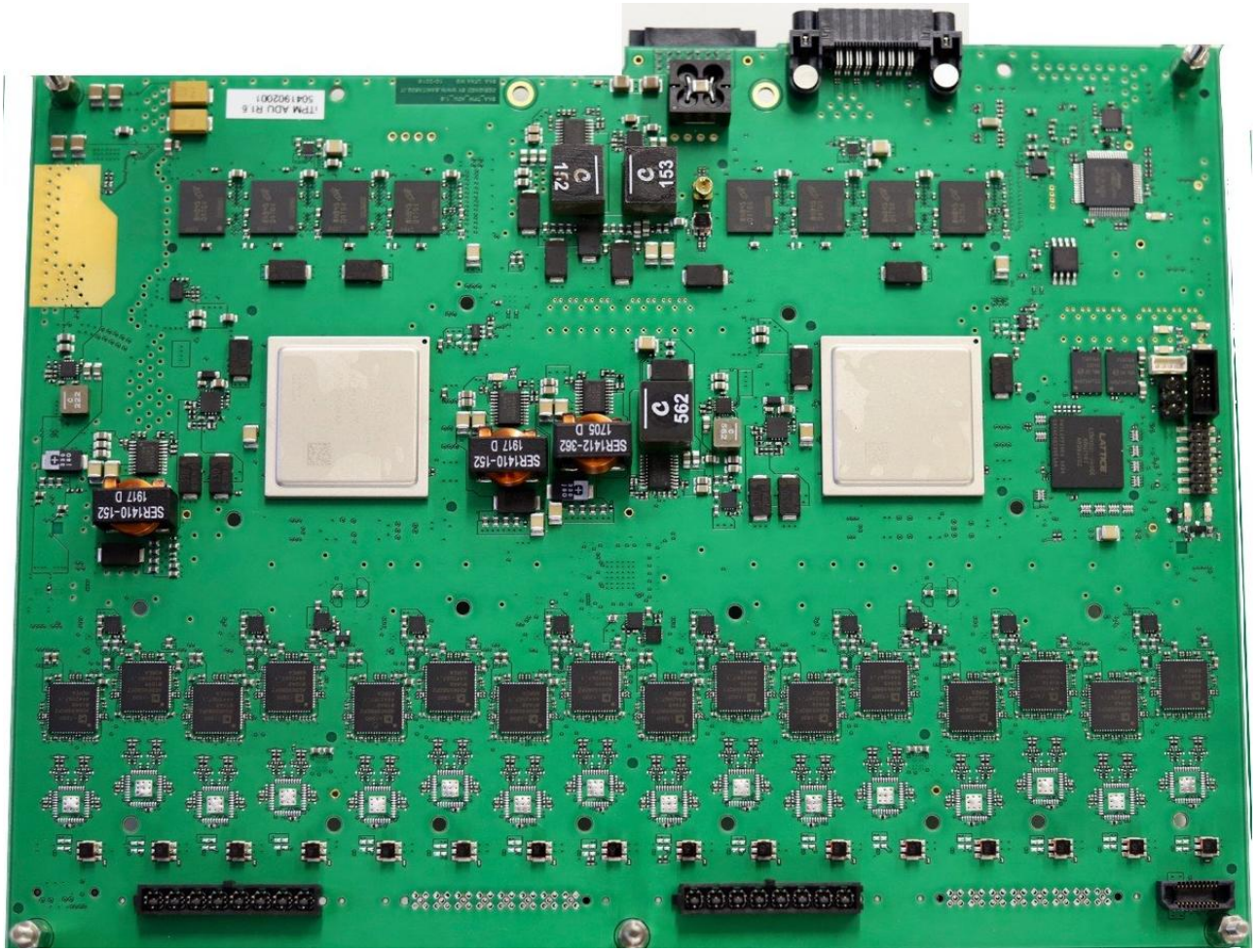


Figure 1. iTPM-ADU 1.6 TOP mechanical layout

The power and management connectors are grouped on one board side, the RF inputs are on the opposite one in Figure 1. The 40G Ethernet QSFP connectors are hosted on a separate board connected with the SAMTEC FLY-OVER cables [RD6].

All the relevant power-dissipating devices are placed on the top side to facilitate the design of a large heat-sink required for the AD devices and the two FPGAs.
A custom heat-sink has been designed for the iTPM-ADU 1.6 Figure 2 , top side and bottom side, optimized for the air cooled LFAA subrack.

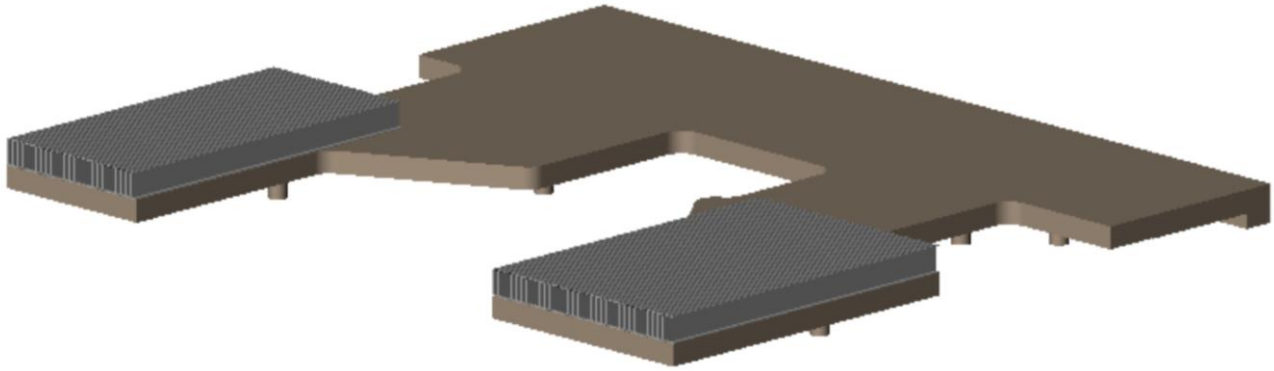


Figure 2. Top heat-sink

iTPM heat-sink provides also electromagnetic shielding of the input RF transformer and protects board analog area from possible damages.
The bottom side heat-sink is mainly for mechanical issue and to complete the transformer shielding on the RF input side with small contribution to the heat dissipation.

The cooling efficiency of the proposed solution is related to the subrack installation of the TPM, including all the plates and fans required to generate the defined air flow around each TPM and the heat-sink in an air cooled rack with an internal temperature range of 20-25°C.

In case of stand-alone usage of the ADU 1.6, an appropriate air flow or specific heat-sink shall be used to guarantee the required thermal management.

The internal subrack design related to the air flow is reported in Figure 3.

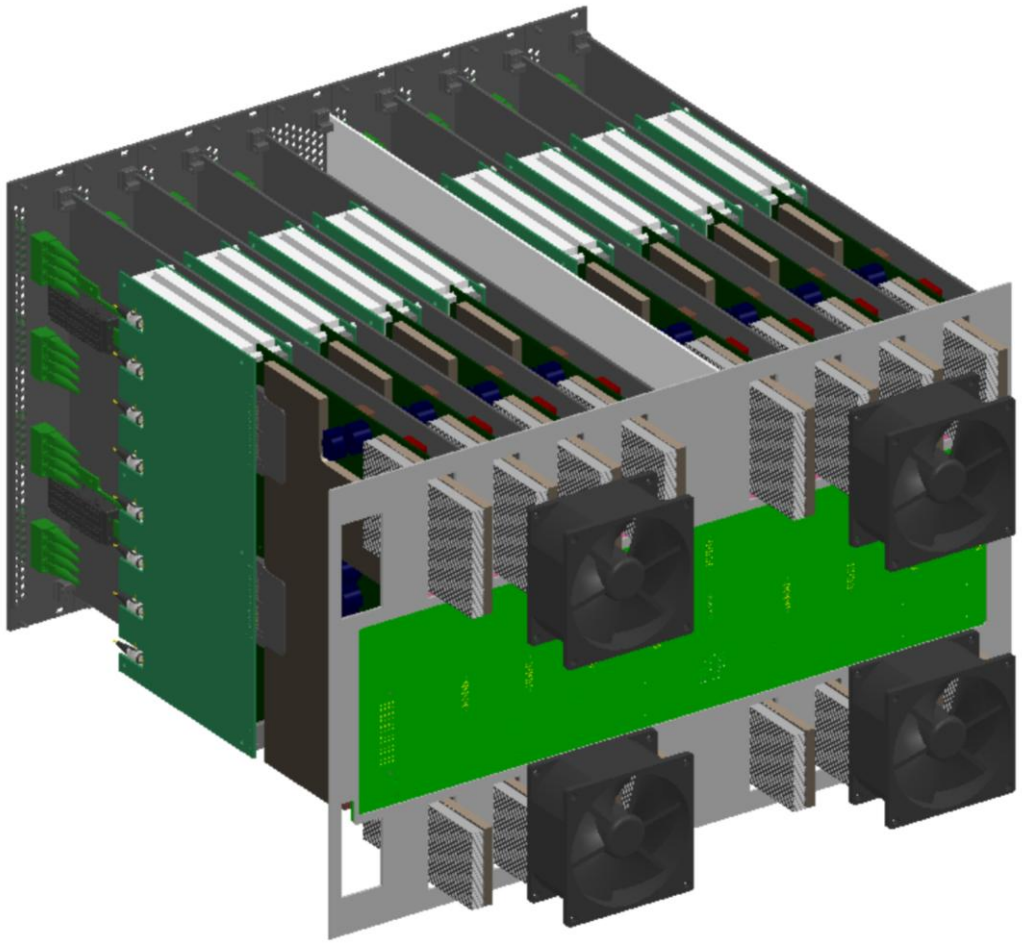


Figure 3 LFAA iTPM internal subrack, air cooling elements

Main components and PCB temperature sensors available on the board shall be monitored to verify correct dissipation. Al the DC-DC converters and the AD converters are protected from internal maximum temperature.

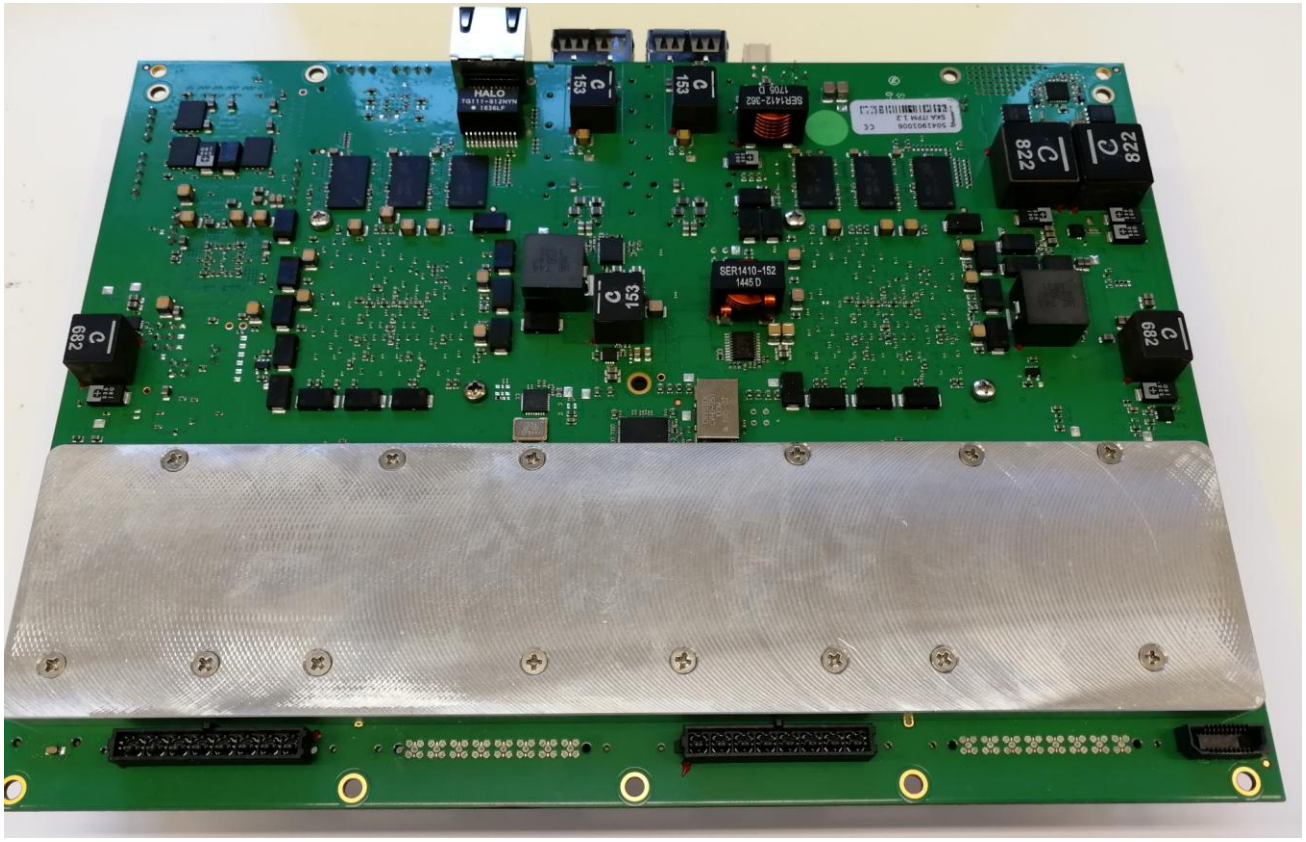


Figure 4 Bottom heat-sink

5.2 Board Layout

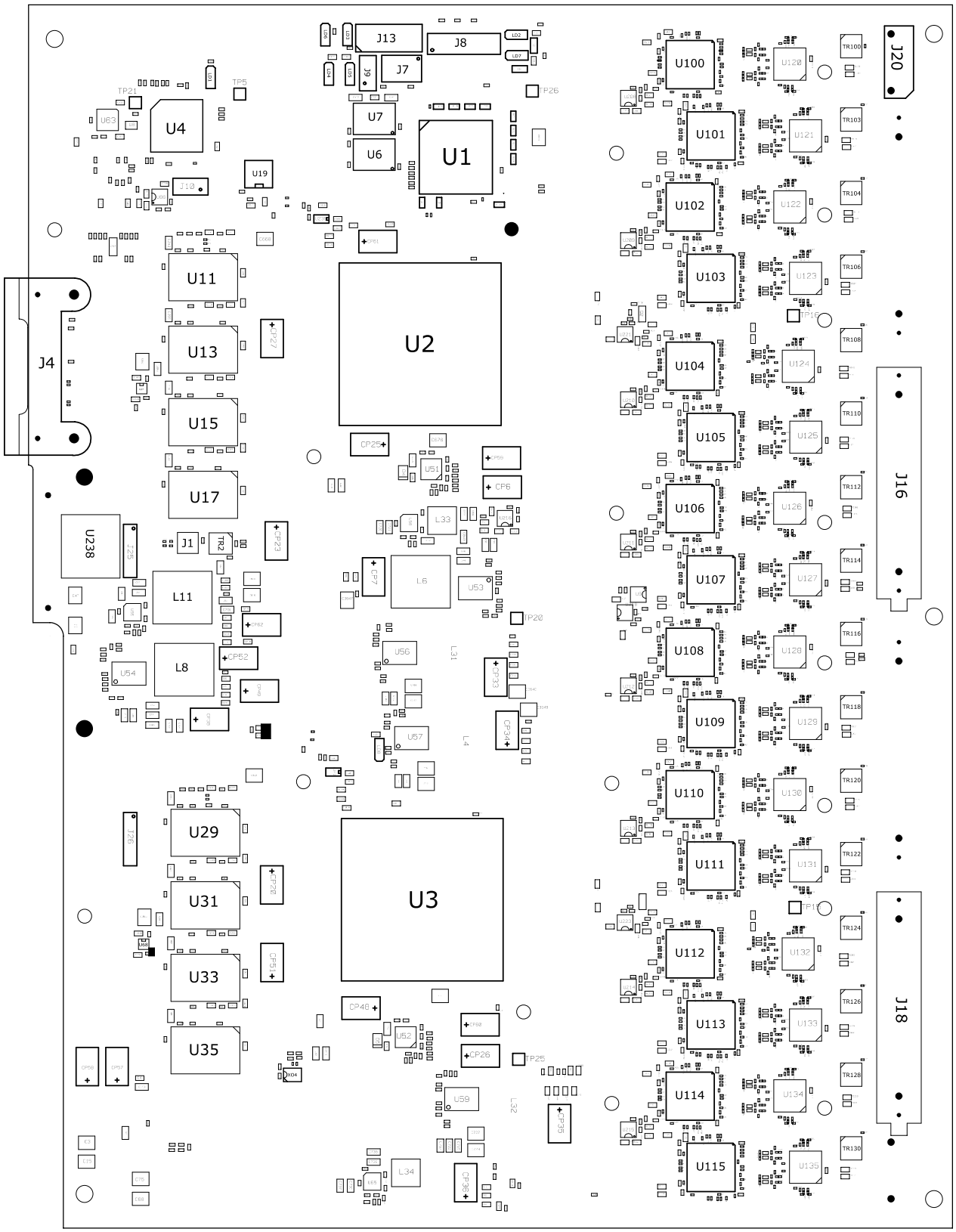


Figure 5. iTPM-ADU 1.6 top placement

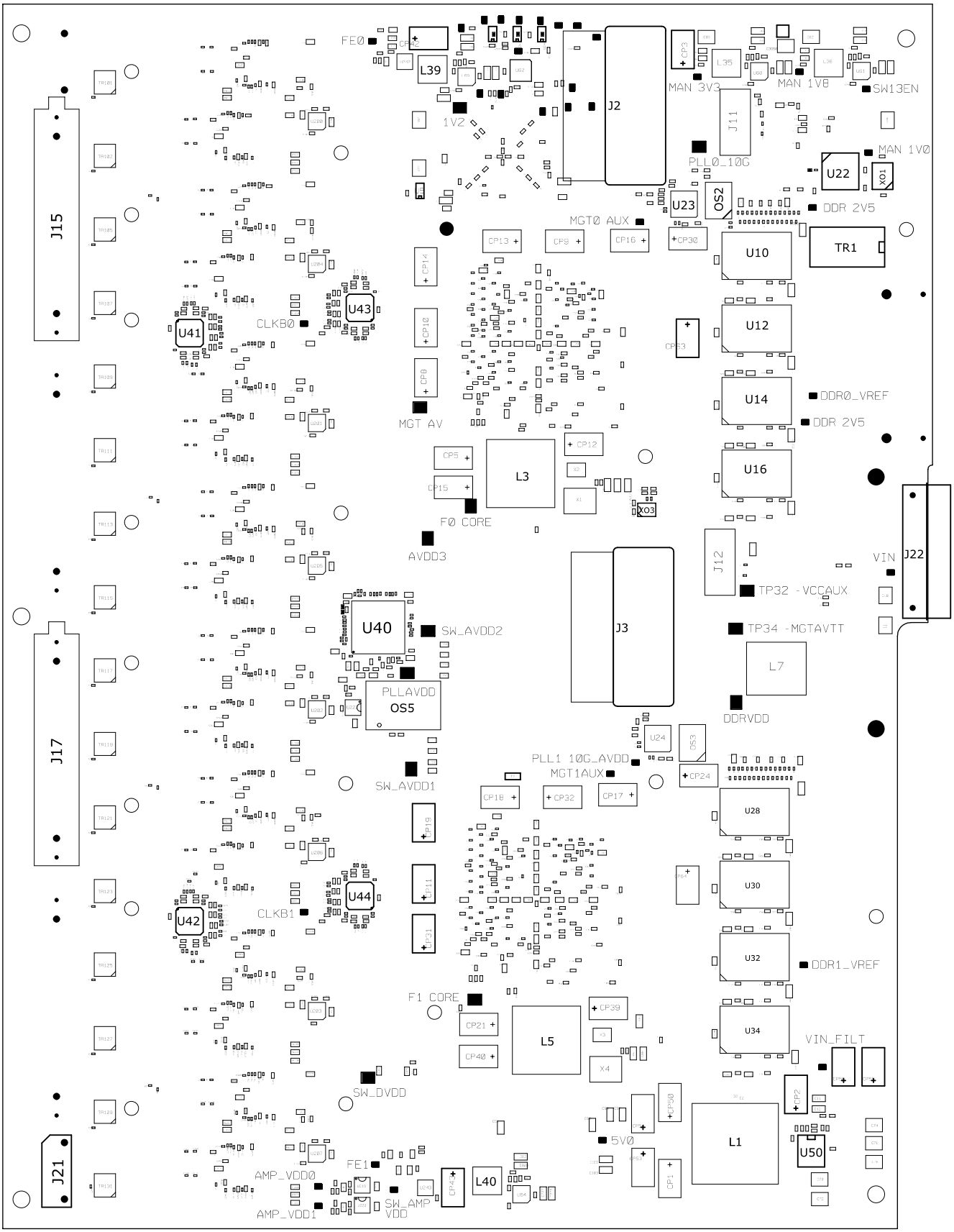


Figure 6. iTPM-ADU 1.6 bottom placement & test points

5.3 Part list, integrated circuits

Reference	Part number	Description
U1	LCMXO3L-9400E-6BG256I	Management CPLD
U2,U3	XCKU9P-1FFVE900E	Main FPGAs
U4	ATSAMD21J18A-AU	Management MCU, ARM Cortex-M0™
U5	24AA025E48	EEprom with pre-assigned MAC
U6,U7	N25Q256A13EF840E	Management SPI 256 Mbit FLASH
U8	ADR5041AKSZ	Linear Supply
U9	ADT7408CCPZ	I2C Temperature sensor
U10-U17, U28- U35	MT40A512M8RH-083	DDR4 application memories, 4 Gbit
U19	MX25R3235FM1IH0	FLASH memory
U22	88E1518-A0-NNB2C000 (TBC)	Management Ethernet transceiver
U23,U24	AD9550BCPZ	10 GE PLL
U40	AD9528BCPZ	Sampling clock generator
U41 - U44	ADCLK948BCPZ	Sampling clock distributors
U50	TPS53355DQP	DDR Vref and Vtt generators
U100 -U115	AD9695BCPZ-1300	Analog to digital converters
U120 - U135	ADL5205ACPZ-R7	Analog amplifiers
U242,U243	ACS70331EESATR-005U3	Current monitor
XO1	ABM3B-25.000MHZ-B2-T	25 MHz oscillator
XO3,XO4	DSC1123CI5-100.0000	100 MHz oscillator

Table 1. iTPM-ADU 1.6 active IC Part list

6. ELECTRICAL CHARACTERISTICS

The following tables show the absolute maximum rating and the recommended operating condition of iTPM-ADU board.

Absolute maximum ratings (*1)					
	Component	**Min**	**Max**	**Units**	**Note**
Input supply	J4	10	16	Volts	Max 150 Watt
PPS in	J22	3	3.5	Volts	Single end signal
Board center temperature (*1)	U9	5	65	°C	ADC PCB max temperature
10 Mhz clock-in	J22				
Front-end digital I/O	J20, J21	3	3.5	Volts	Single end signal
RF input	J15-J18				

Table 2. Absolute maximum ratings

(*1) Device maximum internal temperature shall be guarantee with proper heat sink. FPGA core temperature is function of the firmware application and maximum die temperature shall be verified by the USER in the operative conditions.

Recommended operating conditions					
	Component	**Min**	**Max**	**Units**	**Note**
Input supply	J22	11.5	12.5	Volts	Max 125 Watt
PPS in	J22	3.2	3.4	Volts	
Board center temperature (*1)	U9	5	55	°C	Expected ADC Junction temp. 80°C
10 Mhz clock-in	J22				
Front-end digital I/O	J20, J21	3.2	3.4	Volts	
RF input	J15-J18				

Table 3. Recommended operating conditions

GENERAL NOTES

The TPM ADU rev 1.6 board has been designed for a continuous running with an application that requires about 108W of power consumption and an application specific heat-sink, with FPGA contribute of 28Watt, each, and acquisition running at 800 MHz with 8 bit resolution. In these conditions the internal device operative temperature is guaranteed.

If the FPGA application firmware requires more power and/or the acquisition speed mode is configured at higher speed or resolution, the user shall update the thermal design to respect the temperature recommended conditions.

7. ITPM BLOCK DIAGRAM AND MAIN FUNCTIONS

In this chapter the main iTPM functions are described. First of all, the board block diagram is shown and commented to help identifying which board physical component(s) cope with each function.

7.1 Board Block diagram

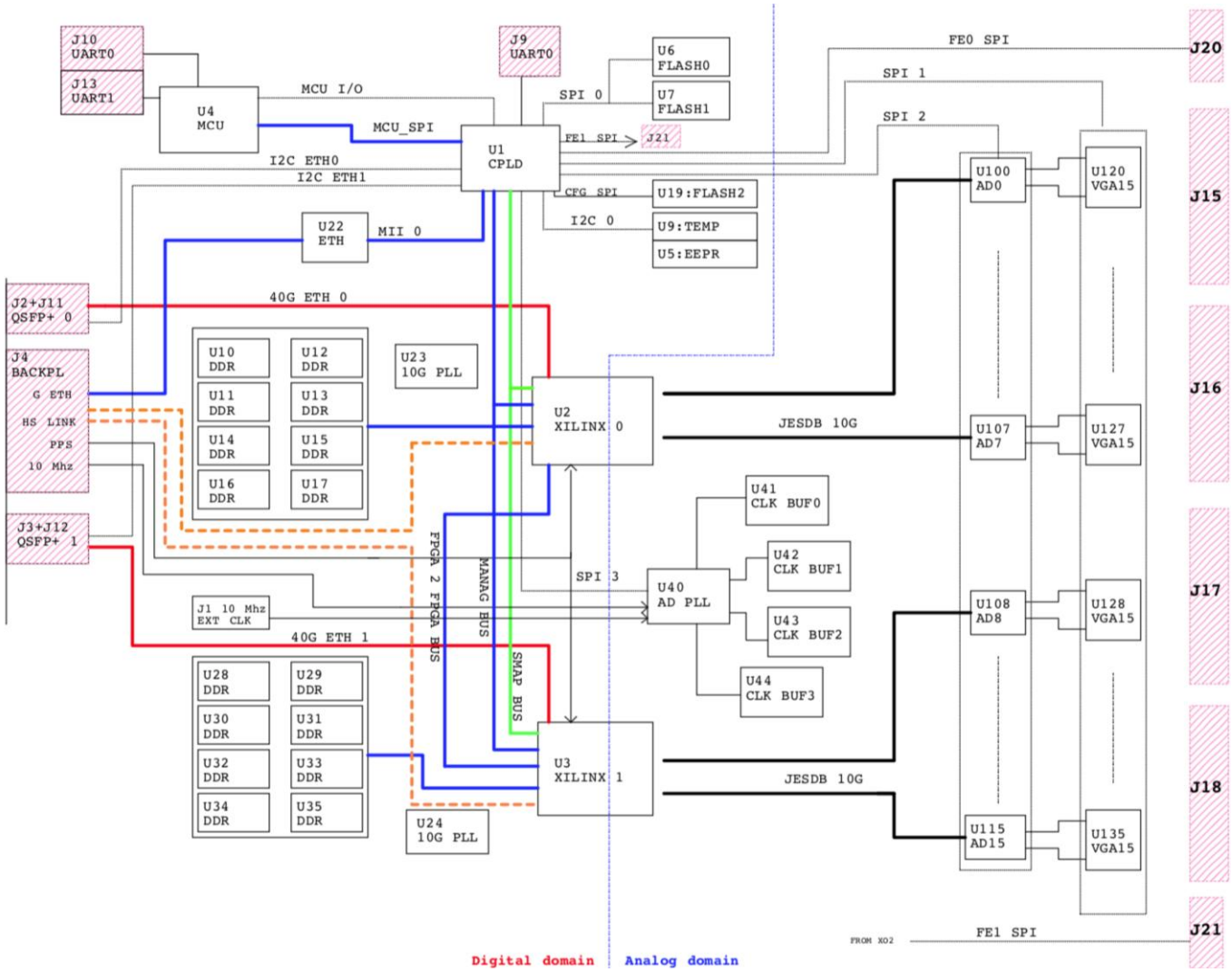


Figure 7. iTPM-ADU 1.6 Block Diagram

The iTPM processor board is organized in three areas, from left to right: management and power supply, FPGA and memories, analog signal interface.
The organization of physical components layout into three separate areas has been adopted to obtain performance and noise isolation between DC-DC converter, digital elements and analog interface.

The **management interface** includes the 10/100/1000 data link, the FLASH based CPLD (U1), the Micro Controller Unit & System Monitor (U4), the SPI FLASH memories (U6, U7) and the CPLD external configuration flash, U19.

The iTPM **FPGAs** are two identical devices (U2, U3), in particular, Xilinx XCKU9P-1FFVE900E that provide suitable and efficient resources to implement all the main board data management and elaboration functions. Each FPGA contributes to the System Monitor function too.

The iTPM **analog section** includes the acquisition clock generation and distribution network (U40, U41 – U44), the sixteen dual channel ADCs (U100-U115), the sixteen dual channel analog buffers (U120-U135) and the four RF high isolation x8 input connectors (J15-J18). Two connectors (J20 and J21) provide supply and digital SPI control for a pluggable analog board for signal over-fiber connection and physical connection.

7.2 Board Management Functions

The iTPM-ADU configuration registers and the device control signals are managed by the CPLD (U1). This device has an internal flash and is auto-configuring at the board start-up. It provides Ethernet user interface and bus lines to connect all the devices configuration interfaces.
The low level CPLD functions can be grouped in upper level function by the MCU that interfaces with a dedicated SPI bus and GPIO with the CPLD.

The management CPLD implements the following bus interfaces:

- RGMII to Ethernet PHY for the remote board control, UDP command interface
- FPGA management bus for USER FPGA register access and debug purpose
- Two independent FPGA SPI buses for device configuration and reconfiguration (FSPI)
- I2C 0, I2C bus connected with a temperature sensor placed in the board hottest area and a 2K bit EEprom for test purpose and board MAC address
- I2C ETH0,1, I2C buses connected with the I/O expander on the FQSFP interface boards
- SPI 0, connected to two identical high speed FLASH memories to store multiple FPGA configuration bitstream and other board non volatile configuration data
- SPI 1, connected with clock, enable and data decoded to configure the 32 Analog amplifiers
- SPI 2, connected with clock, enable and data decoded to configure the 16 Analog to Digital converters
- SPI 3, connected with acquisition PLL
- MCU SPI, slave, connected with MCU
- MCU GPIO to implement direct connection and interrupt signals
- UART on a user connection for debug purpose
- External Xilinx JTAG Interface
- Two Internal Xilinx JTAG Interfaces, one for each device

The management user interface is based upon the Ethernet-UDP IP core, which allows executing sequences of memory mapped bus accesses from a remote console. On board MCU can access through a SPI direct access to the CPLD and execute direct memory access to the internal bus.

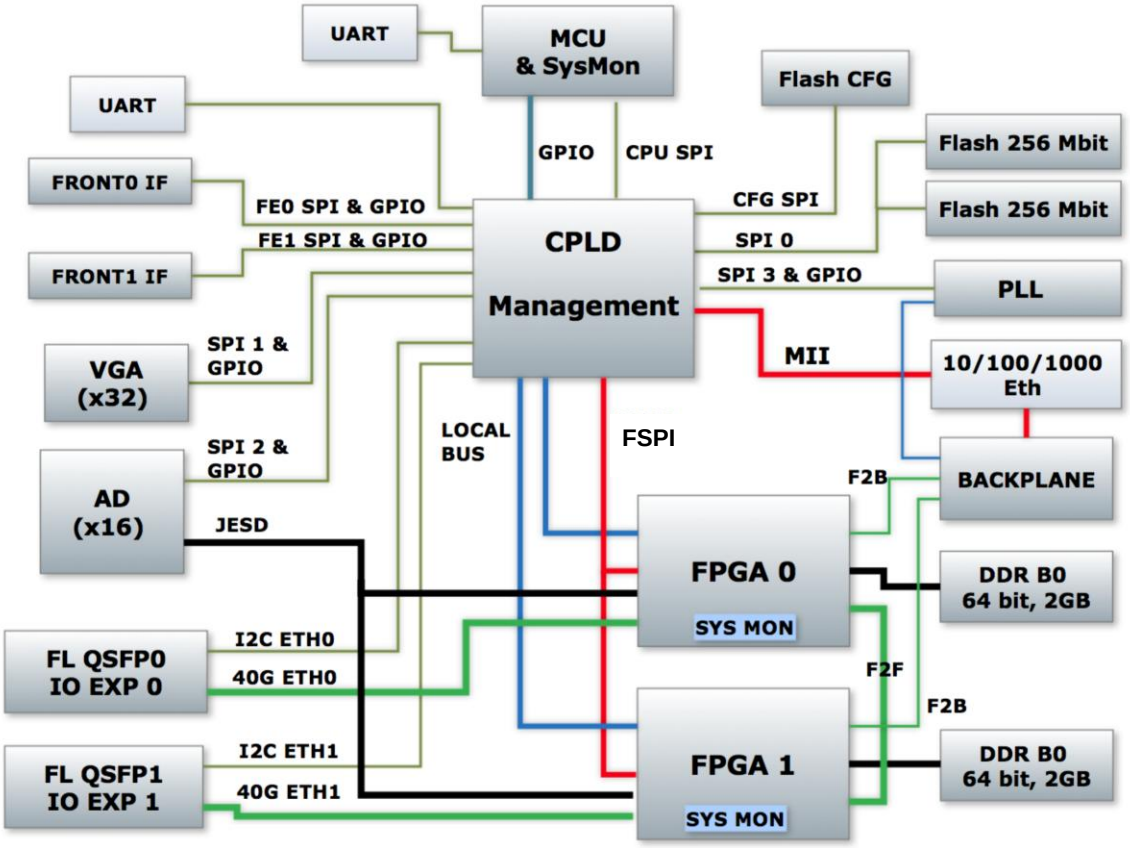


Figure 8. CPLD management interfaces

The Board Control and Monitoring functions are shared between the CPLD device, the MCU device and the FPGA devices. The CPLD implements the time critical control operations while the MCU and FPGAs the monitoring functions.
The CPLD control pin list is the following, [RD2]:

PIN n°	Pin Function	ADU 1.6 NET	EXPECTED VALUE
M6	POWER FPGAS	EN_FPGA	1
N6	POWER ADC	EN_ADC	1
L9	POWER PLL & VGA	EN_VGA	1
N8	POWER FRONT END	EN_FE	1
N11	POWER SYSREF DISTR	EN_SYSR	1

Table 4. CPLD supply control pin

The management CPU is a low power 32 bit, 48 MHz ARM Cortex M0+ core, integrating 256 Kbyte of internal FLASH and a 32 Kbyte RAM memory. The CPU is connected with the CPLD with an SPI link and GPIOs. The CPLD firmware provides communication links to and from external board control application and register level access to all the board configuration registers and management memory areas.

Clock and reset signals are generated by the CPLD after power on. The CPU is connected with board resources through the management CPLD.

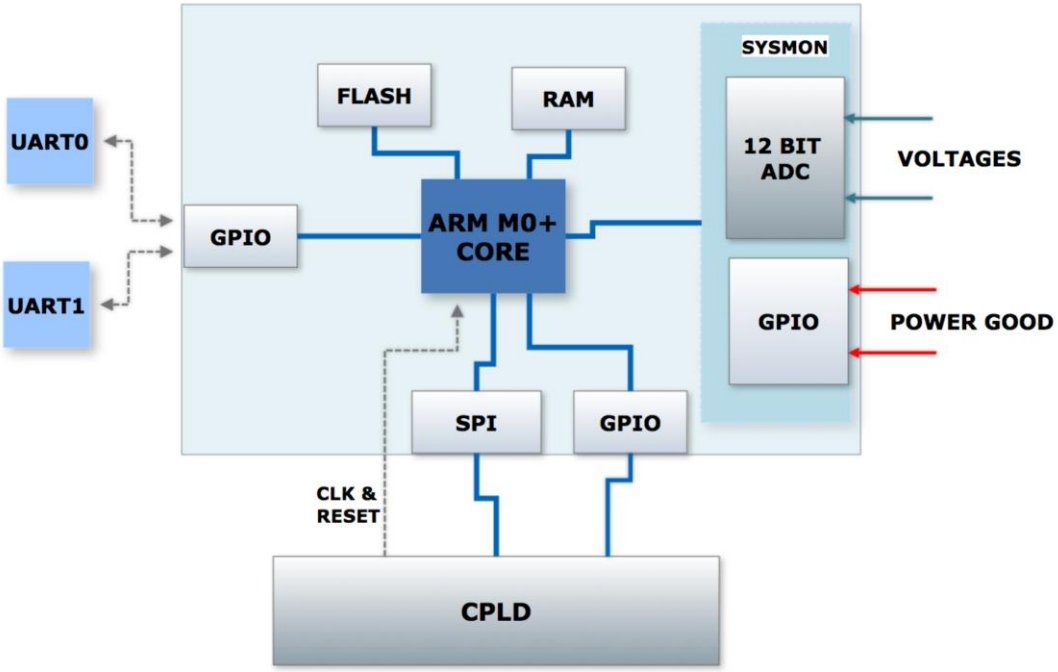


Figure 9. iTPM-ADU 1.6 management CPU

The MCU monitoring functions exploit the voltage monitoring of the primary DC-DC converters with the internal 12 bit ADC module and check the power good status signal of the same DC-DC converters that in case of failures lowers a dedicated output pin.

The MCU Monitor signals on the ADU 1.6 are listed in the following table:

PIN n°	Pin Function	ADU 1.5 NET
	ANALOG INPUTS	
3	AIN0	SAM_DAC
4	AIN1	VREF 2,5V
5	AIN2	MON_DDR2V5
6	AIN3	-
9	AIN4	MGT_AVcc
10	AIN5	MGT_AVtt
11	AIN6	-
12	AIN7	-
13	AIN8	SW_AVDD1
14	AIN9	SW_AVDD2
15	AIN10	AVDD3
16	AIN11	MAN_1V2
17	AIN12	DDR0_VREF
18	AIN13	DDR1_VREF
19	AIN14	VM_DRVDD
20	AIN15	-
61	AIN16	VIN_SCALED
62	AIN17	MON_3V3
63	AIN18	MON_1V8

64	AIN19	MON_5V0
	DIGITAL INPUTS	
42	IO19	PG_FPGA
45	IO22	PG_FE
46	IO23	PG_AVDD
59	IO30	PG_MAN
60	IO31	PG_ADC

Table 5. MCU Monitor signals

The MCU ADC can be scaled on the internal 1V reference or to the external 2,5V reference provided on the board. Reference scales shall be selected to match the expected maximum monitored voltages.
The MCU provides also a Digital to Analogue Output, available on a test point, TP21. On the board all the Power Good signals are pulled up to 3v3 Vcc.

FPGA SYSMON feature completes the management monitoring capabilities: each FPGA provides sixteen analog inputs that are connected internally with the FPGA supplies and externally with the board supply and the front-end current sensors. FPGA SYSMON registers shall be accessed with the FPGA local bus or the JTAG interface.
FPGA external system monitor connections on the ADU 1.6 are the following:

PIN n°	Pin Function	ADU 1.6 NET
FPGA 0		
AC22	AD2	FE0_MVA
AH24	AD8	VM_ADA0
AK23	AD9	VM_ADA1
AC23	AD1	VM_AGP0
AD24	AD4	VM_AGP1
AG23	AD7	VM_AGP2
AH22	AD10	VM_AGP3
AE22	AD5	VM_CLK0B
AC21	AD3	VM_DDR0_VTT
AB23	AD0	VM_FE0
AF22	AD6	VM_MGT0_AUX
AJ22	AD11	VM_PLL
FPGA 1		
AH24	AD8	FE1_MVA
AC22	AD2	VM_AGP4
AB23	AD0	VM_AGP5
AC21	AD3	VM_AGP6
AD24	AD4	VM_AGP7
AC23	AD1	VM_CLK1B
AJ22	AD11	VM_DDR1_VDD
AF22	AD6	VM_DDR1_VTT
AG23	AD7	VM_DVDD

AK23	AD9	VM_FE1
AE22	AD5	VM_MGT1_AUX
AH22	AD10	VM_SW_AMP

Table 6. FPGA SYSMON signals

The ADU 1.6 has three I2C buses; I2C0 connected on board temperature sensor and EEprom; I2C ETH0, I2C ETH1 connected each to one of the FQSFP extension board that provides the connection with the 40G QSFP cable interface and an I/O expander that manages the QSFP static control signals and four Front Panel LEDS [RD9].

BUS	Device	Address	Description
I2C 0	U9	0011 000	12 bit temperature sensor
	U5	1010 000	2 Kbit EEprom
10GE0,1 I2C	FQSFP- J2	1010000	QSFP standard I2C address
	FQSFP- U1	0100000	IO EXPANDER address

Table 7. iTPM-ADU 1.6 I2C Device Addresses

Two High Speed SPI flash memories are connected to the same SPI 0 bus (U6,U7) and activated by separated chip select lines; these memory devices can store several FPGA configuration bitstreams and other management data.

Device	BUS	Selection
U6	SPI 0	MAN_SPI0_CS0_N
U7		MAN_SPI1_CS0_N

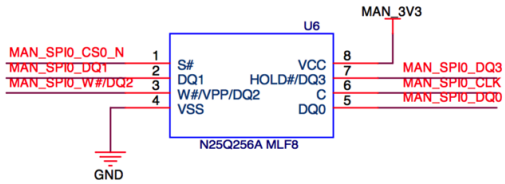


Figure 10. SPI0 bus connections

Ethernet I/F is structured with MII interface routed to a CPLD MAC and UDP core that decodes the Ethernet packets to the CPLD internal memory space where shall be mapped all the ADU1.6 low level management functions.

Slave serial I/F is connected from the CPLD to the FPGA configuration interface (FSPI); data bus is dedicated for each device, to allow independent configuration and configuration speed up to 125 Mbps.

CPLD PIN	FPGA PIN	Pin Function	ADU 1.6 NET
	FPGA 0		
R16	AD25	DIN	XIL0_D0
P16	AG26	CCLK	XIL0_CCLK
	FPGA 1		
N16	AD25	DIN	XIL1_D0
M16	AG26	CCLK	XIL1_CCLK

Table 8. Slave serial signals

Local bus interface extends the management bus from the CPLD to the two main FPGAs for management and debugging. A direct RGMII like bus from each FPGA to the system monitor to upload data at Ethernet full speed.
Memory mapped bus is an 8 bit address/data with CLOCK, RESET and ACK signals. RGMII bus is 4 bit data with a CLOCK, Control and a STROBE each.

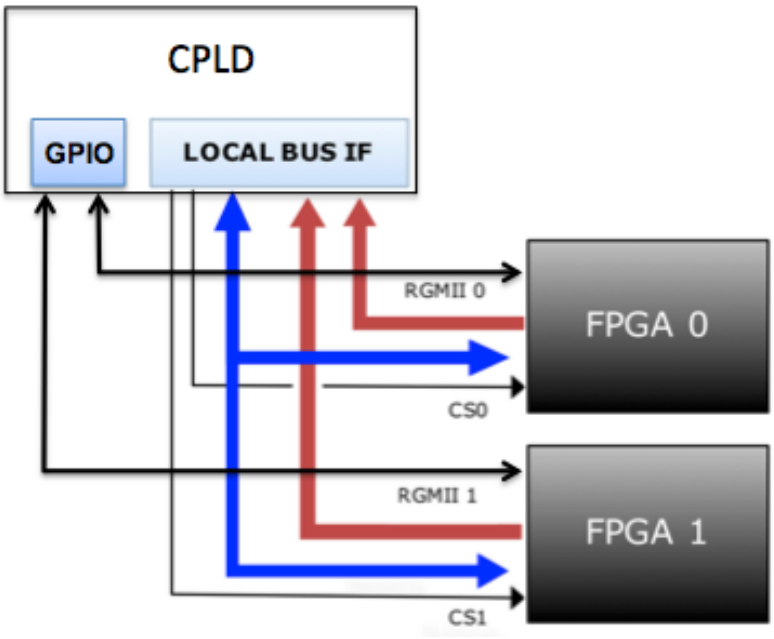


Figure 11. Management local bus structure

From each FPGA, two GPIO signals are connected directly to the CPLD (XIL_CPLD).

The management components have dedicated supply and are instantly active at the board power-on. Management devices shall manage the DC-DC converters to execute the board power-on procedure and configure the board for the required operations. Maximum current, internal generated voltages and temperature monitors information are always available for on-board verification and safety.

7.3 Power Distribution and Monitor Functions

iTPM power supply and monitoring is a complex structure organized in several sections.

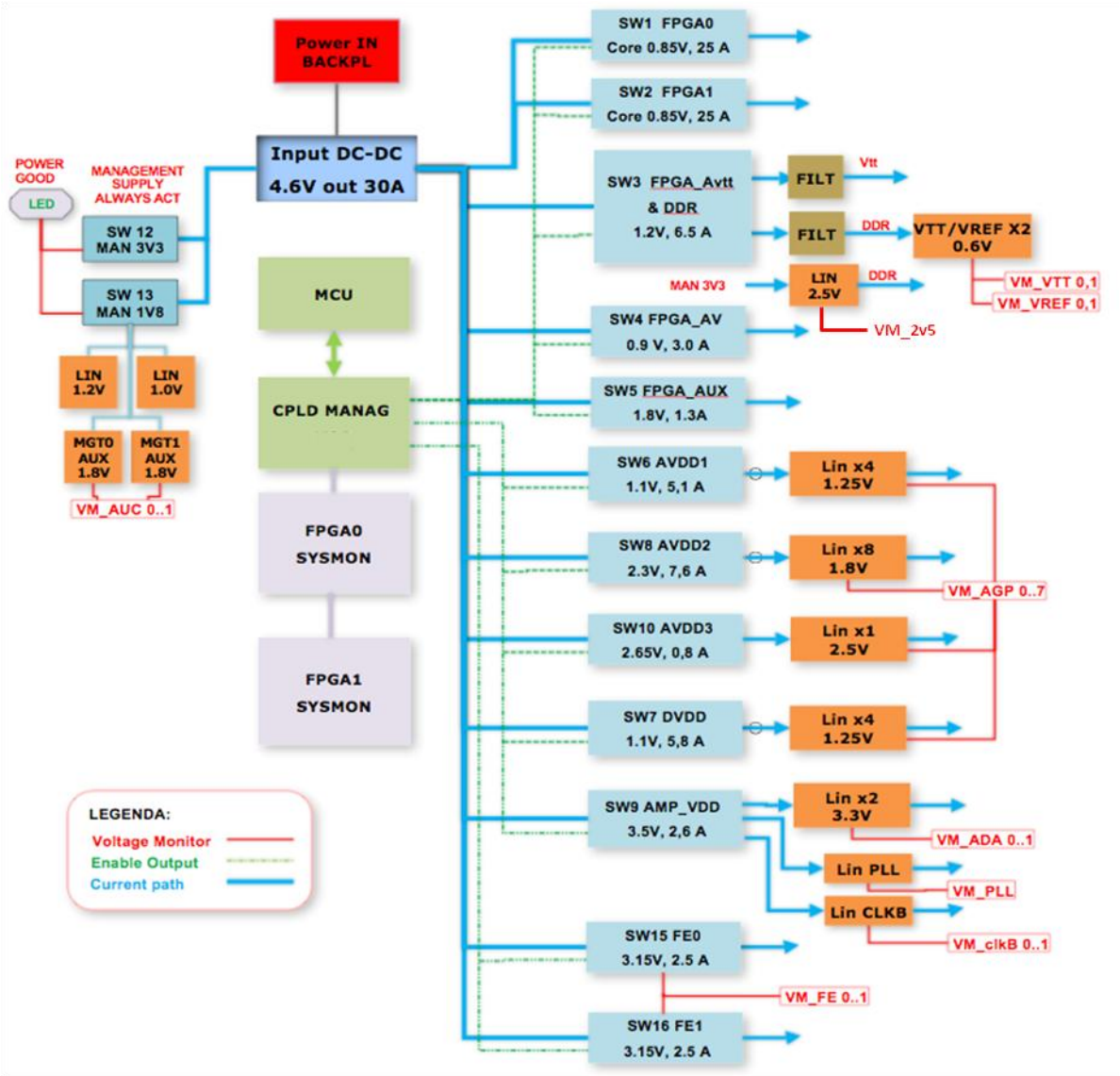


Figure 12. iTPM-ADU power supply and monitoring block diagram, nominal values

The first section includes the ALWAYS ON devices, i.e. each management device except for the voltage monitor inside the main FPGA.
Input voltage is reduced from 12V to the internal 4.6V (max 30A) and is distributed to all the second level DC-DC voltage converters. Three management DC-DC devices are always active to supply the CPLD, System Monitor, MCU, Flash and Ethernet interface. System Monitor and CPLD can check input current and enable each second level DC_DC converter to supply all board devices. By default all devices are disabled: at power on only the management functions are active.

The other sections deal with the devices based on their functions: there is one section for the FPGAs and the DDR memories, one for the devices involved on Analog to Digital conversion,

one for the analogue amplifiers and PLLs and the last one to supply the external analogue front end. Each section is supplied by one or more DC-DC converters, and each DC-DC has separate slew rate control so as proper sequence and voltage monitoring shall be executed.

High quality analog interfaces, AD, PLL and Amplifier, are isolated and filtered by low noise and high PSRR linear regulators and ferrites to eliminate common mode supply noise effects.
In addition two DC-DC converters are provided to supply the expansion board that can be connected to the RF input connector; these DC-DC converters shall be enabled and a current monitor is present on each output to calculate effective iTPM power needs in nominal operation.

To power-on the board, the appropriate DC-DC supply generator shall be connected to the backplane J22 connector, up to 140 Watt 12 V DC supply shall be applied.
J22 schematics and BOTTOM layout are below:

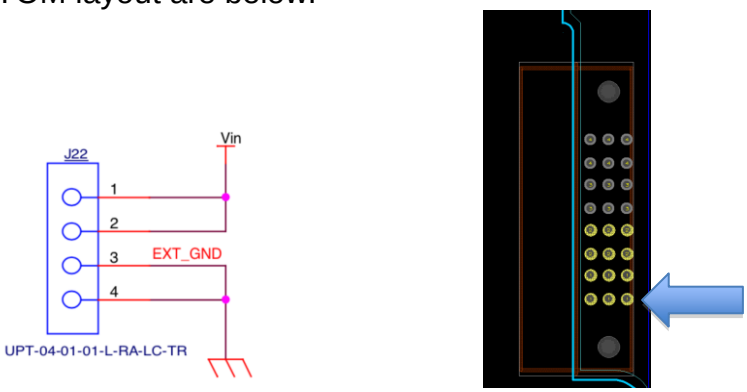


Figure 13. J22 Power connector, bottom view, arrow on pin 1

To measure the input voltage, System Monitor maximum input voltage (3,3V) shall be respected. On board resistor scaled the input voltage to be safely measured.



Figure 14. Input voltage scaling for measurement

On board power and voltage monitoring is provided. The following points of measure are accessible by the management interface:

- Input voltage value
- Internal 5V voltage value
- Internal 5V generated current, corresponding to the total board absorbed Power after the first DC-DC input converter
- Internal voltage generated by all the DC-DC converter
- Output current generated for each expansion connector (to calculate the effective iTPM absorbed power)

- Cumulated voltage monitor for each AD linear regulator set. Two ADs are supplied by a linear regulator set. The generated supply are joined by resistors and a defined voltage value can be verified
- Linear voltage generated for analog devices

Current and voltage monitors are provided by the System Monitor (U5) and the FPGAs System Monitor function (U2, U3). The voltages measured by the FPGA can be accessible by the user registers interface in the programmed device (IP core is required).

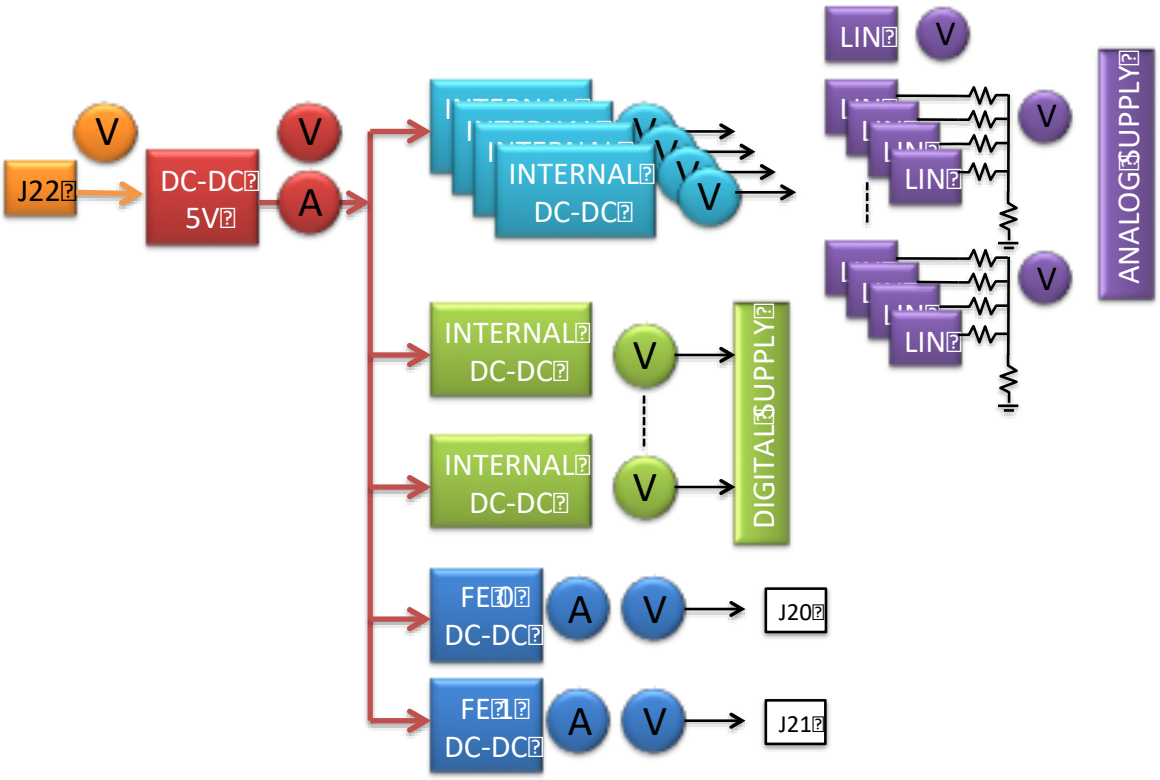


Figure 15. iTPM voltage and current points of measure

All the iTPM-ADU 1.6 DC-DC supply components are individually monitored but some of the analogue linear regulator are grouped to reduce the required number of monitor measurement inputs.

MCU (U4) voltage monitor input accepts a range, 0-2,5 V and FPGA ADC work in the range 0-1,2 V so voltage scaling is provided with following resistors:

Voltage type	V IN (V)	R1 (KΩ)	R2 (KΩ)	V OUT (V)
VM_SW_AMP	3,5	20	4,53	0,65
VM_3V3	3,3	31,6	11,5	0,88
VM_3V15	3,15	31,6	11,5	0,84
VM_DVDD	1,1	4,99	10,2	0,74
VM_1V8	1,8	20	11,5	0,66
VM_1V2	1,35	4,99	10,2	0,81

Table 9. Resistors for voltage scaling

DDR_VTT is managed by FPGA memory interface: it shall be enabled before measuring it. Other supplies are enabled directly by the management.

The sixteen ADs are grouped in eight couples for supply; each group of two ADs is supplied by four linear regulators. The regulator outputs are combined and scaled, to cope with their large number. The calculated value of the eight VM_AGPi signals shall be used to check the supply values.

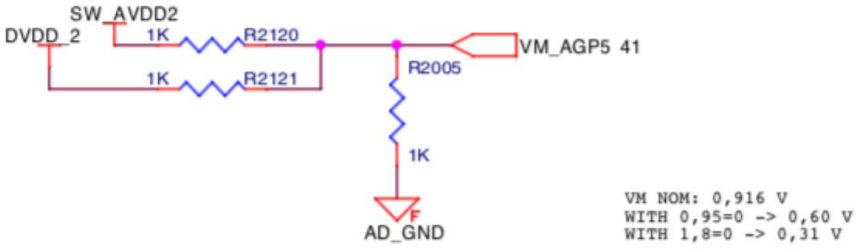


Figure 16. Scaled voltage AD group 2

iTPM-ADU complete voltage and temperature points of measure and expected values are listed in the tables below.

The following four temperature sensors are available:

Sensor Position	Description
MCU	Inside the MCU itself; it is the only temperature measurement available when nothing else is powered on
FPGA 0	Inside FPGA, connected to the System monitor
FPGA 1	Inside FPGA, connected to the System monitor
PCB, close to ADC	I2C temperature sensor (U245) placed in the board center, in the expected worst temperature board position in operative mode.

Table 10. Temperature points of measure

The following tables list the available Voltage points of measure. In the MCU System Monitor table the supplies status are listed too.

MCU SYSTEM MONITOR						
PIN n°	Pin Function	ADU 1.6 NET	EXPECTED VAL	VREF	Tolerance	Description
	ANALOG INPUTS					
3	AIN0	SAM_DAC			-	DAC Output
4	AIN1	VREF 2,5V	2,5	-	-	Externel ADC reference
5	AIN2	-				
6	AIN3	-				
9	AIN4	MGT_AVcc	0,9	1,0	3%	FPGA MGT AV
10	AIN5	MGT_AVtt	1,2	2,5	3%	FPGA MGT AVTT
11	AIN6	-				
12	AIN7	-				
13	AIN8	SW_AVDD1	1,1	2,5	3%	SW Analog 1,1 V
14	AIN9	SW_AVDD2	1,95	2,5	3%	SW Analog 1,95 V
15	AIN10	AVDD3	2,5	2,5	3%	Analog 2,5 V
16	AIN11	MAN_1V2	1,2	2,5	5%	Management 1,2V
17	AIN12	DDR0_VREF	0,6	1,0	3%	DDR 0 Vref voltage
18	AIN13	DDR1_VREF	0,6	1,0	3%	DDR 1 Vref voltage
19	AIN14	VM_DRVDD	1,8	2,5	3%	SW DRVDD 1,8V voltage
20	AIN15	-				
61	AIN16	VIN_SCALED	2,09	2,5	5%	Input supply voltage
62	AIN17	MON_3V3	1,65	2,5	5%	Management 3,3V
63	AIN18	MON_1V8	1,25	2,5	5%	Management 1,8V
64	AIN19	MON_5V0	1,83	2,5	5%	Internal 4,6 V supply
	DIGITAL INPUTS					
42	IO19	PG_FPGA	HIGH			Power Good FPGA supplies
45	IO22	PG_FE	HIGH			Power Good Front End supplies
46	IO23	PG_AVDD	HIGH			Power Good ADC Linear supplies
59	IO30	PG_MAN	HIGH			Power Good Management supplies
60	IO31	PG_ADC	HIGH			Power Good ADC DC-DC supplies

Table 11. MCU Voltages and status points of measure

FPGA SYSTEM MONITOR						
PIN n°	Pin Function	ADU 1.6 NET	EXPECTED VAL	VREF	Tolerance	Description
FPGA 0						
AC22	AD2	FE0_MVA	TBD	1,2		FE0 Absorbed current, 400 mV/A
AH24	AD8	VM_ADA0	0,88	1,2		AMP VDD0 3,3V voltage
AK23	AD9	VM_ADA1	0,88	1,2		AMP VDD1 3,3V voltage
AC23	AD1	VM_AGP0	0,916	1,2		AD AGP group 0 Voltage Monitor
AD24	AD4	VM_AGP1	0,916	1,2		AD AGP group 1 Voltage Monitor
AG23	AD7	VM_AGP2	0,916	1,2		AD AGP group 2 Voltage Monitor
AH22	AD10	VM_AGP3	0,916	1,2		AD AGP group 3 Voltage Monitor
AE22	AD5	VM_CLK0B	0,88	1,2		Clock Buffer0 3,3V Voltage Monitor
AC21	AD3	VM_DDR0_VTT	0,6	1,2		DDR FPGA0 Vtt Voltage Monitor
AB23	AD0	VM_FE0	0,84	1,2		FE0 Voltage Monitor
AF22	AD6	VM_MGT0_AUX	0,65	1,2		FPGA MGT0 AUX Voltage Monitor
AJ22	AD11	VM_PLL	0,88	1,2		ANALOG PLL Voltage Monitor
FPGA 1						
AH24	AD8	FE1_MVA	TBD	1,2		FE1 Absorbed current, 400 mV/A
AC22	AD2	VM_AGP4	0,916	1,2		AD AGP group 4 Voltage Monitor
AB23	AD0	VM_AGP5	0,916	1,2		AD AGP group 5 Voltage Monitor
AC21	AD3	VM_AGP6	0,916	1,2		AD AGP group 6 Voltage Monitor
AD24	AD4	VM_AGP7	0,916	1,2		AD AGP group 7 Voltage Monitor
AC23	AD1	VM_CLK1B	0,88	1,2		Clock Buffer1 3,3V Voltage Monitor
AJ22	AD11	VM_DDR1_VDD	0,81	1,2		DDR4 Voltage Monitor
AF22	AD6	VM_DDR1_VTT	0,6	1,2		DDR FPGA1 Vtt Voltage Monitor
AG23	AD7	VM_DVDD	0,74	1,2		AD DVDD Voltage Monitor
AK23	AD9	VM_FE1	0,84	1,2		FE1 Voltage Monitor
AE22	AD5	VM_MGT1_AUX	0,65	1,2		FPGA MGT1 AUXVoltage Monitor
AH22	AD10	VM_SW_AMP	0,65	1,2		VGA DC-DC Voltage Monitor

Table 12 FPGAs Voltages

WARNING: iTPM-ADU is a high density board with relevant absorbed power. External heat cooling system is required and continuous temperature monitoring shall be done to verify to not exceed maximum component temperature.

Board management components implement a protection mechanism based on threshold values to partially switch-off the board components and limit severe damages.

Warning thresholds can be modified in the management system to generate a system alarm

---

ITPM-ADU board revision 1.6 provides this power optimization feature: separable supply for the two clock buffer drivers that distribute the JESD SYSREF signal to all AD devices. Since this signal is required only to synchronize the first acquisition on the same clock edge for all the ADs, the corresponding PLL output and clock buffer shall be disabled during continuous acquisition (EN_SYSR). About 1Watt power is required to generate and distribute these signals.

7.3.1 iTPM Power Budget

iTPM board total internal absorbed power shall not exceed 125Watt due to current limitation of the 5V internal supply generator. Maximum power for all DC-DC converters shall also be respected. In the LFAA subrack configuration, the total absorbed supply is monitored at backplane level and only the Front End current supply can be monitored to verify that the user application respects the power budget.
DC-DC capability and expected load are shown in Table 13; nominal current is the total calculated current of the load in a typical configuration.

iTPM DC-DC capabilities				
	Output Voltage	**Current, nominal**	**Current, MAX**	**LOAD**
Input DC_DC	4,9V	30A	34A	All internal DC-DC supply
SW 1	0,85V	25A	30A	FPGA0 core
SW 2	0,85V	25A	30A	FPGA1 core
SW 3	1,2V	6.5A	12A	FPGA MGT AVTT & DDR4
SW 4	0,9V	3A	12A	FPGA MGT AV
SW 5	1,8V	1,3 A	4A	FPGA MGT AUX
SW 6	1,1V	5,1A	12A	AD AVDD1
SW 7	1,1V	5,8A	12A	AD DVDD
SW 8	2,3V	7,6A	12A	AD AVDD2
SW 9	3,5V	2,6A	4A	AMP VDD
SW 10	3,5V	0,8A	4A	AD AVDD3
SW 12	3,3V	0,8A	4 A	Management 3,3V, QSFP+
SW 13	1,8V	1,2A	4A	Management 1,8V
SW 15	3,15V	2,5A	4A	FRONT END0 SUPPLY OUT
SW 16	3,15V	2,5A	4A	FRONT END1 SUPPLY OUT

Table 13. DC-DC capability and expected load

Each of the two DC-DCs of FPGA cores (SW1, SW2) can produce up to 30A; the devices are limited to 35A for circuit protection. The others DC-DCs are limited or protected but the exact values are not available.

Expected iTPM power budget in the SKA configuration is presented in Table 14.

iTPM SKA configuration power budget		
Board R1.6		
	ADA	NO ADA
CPLD, Eth, Flash (W)	3	3
MCU (W)	0,5	0,5
STATIC (W)	1,12	1,12
IP DATA ACQ (W)	10	10
DDR (W)	2,04	2,04
CORE (W)	26	26
Local bus, clocks (W)	1	1
40 G Ch 0 (W)	1,25	1,25
40 G Ch 1 (W)	1,25	1,25
PLL, CLKBuff, 10G Pll (W)	3,6	3,6
AD (W)	19,2	19,2
ADA (W)	16	0
Front END (W)	10,6	16,7
TOTAL DIGIT IC (W):	46,9	46,9
TOTAL ANALOG IC (W)	59,4	48,0
TOTAL int 5V supply (A)	21,3	19,0
TOTAL Supply (W)	**112,0**	**100,0**
Absorbed 12V (A)	9,3	8,3
Absorbed 24V (A)	4,7	4,2

Absorbed 32V (A)	3,5	3,1
Assumed efficiency		
Digital DC-DC efficiency:	94%	
Analog efficiency (8%):	86,48%	
Input DC-DC eff:	95%	

Table 14. Expected iTPM power budget in the SKA configuration

The required front-end power is related to ADA/NO ADA board configuration; it is expected that each SKA Analog fiber receiver board power requirement is about 16 Watt when final amplification is required, about 10 Watt in the other case.
Total Supply is the total absorbed power at the J22 connector; DC-DC and linear regulator efficiency has been considered in total supply calculation.
FPGA firmware design and AD configuration specification shall take into account the power requirement in iTPM REV 1.6.

7.3.2 Measured iTPM Rev 1.6 power consumption

The following configurations have been measured in the test-cases for the 1.6 board version, without the Analog Front-End, under these operative conditions:

- Power Input: 12V
- TPM BIOS: v0.0.3 (CPLD_0x20011611-MCU_0xb0000010_0x0_0x0)
- TPM FPGA FW: tpm_test (0x1021737)

Test phase	Power (W)	Active part
Power ON	3,99	Management
Digital supply ON (FPGA not programmed)	6,00	Only digital side powered ON, FPGA not programmed, PLL off
Digital supply ON (FPGA programmed)	18,89	Only digital side powered ON, FPGA programmed, PLL off
All supply ON	17,90	All supply active, FPGA not programmed
All ON, FPGA programmed	32,29	FPGA programmed
Acquisition	64,91	32 channel active at 800 Ms/sec
Acquisition & Elaboration	na	32 channel active at 800 Ms/sec, channelizer firmware

Table 15: iTPM 1.6 power consumption

Measured power is greatly dependent from board temperature and ambient temperature. Proper air flow shall be provided and maximum board and component temperature shall be monitored.

Stable temperature and power condition shall be verified for each acquisition.

Thermal and power stability SHALL be guaranteed for each possible variation of FPGA firmware, AD setting, ambient temperature and air flow speed.

Board center temperature (U9 temperature sensor) and FPGA core temperature shall be monitored.
Board center temperature measures the PCB temperature in the ADC area under the heat-sink; its value shall not exceed 65°C for proper ADC operating conditions.
FPGA maximum temperature is defined in component datasheet and can be measured with internal sensor diode connected with FPGA SYSMON.

7.4 Acquisition and processing Function

iTPM acquisition data path is organized in four sections: the analog to digital conversion, the data elaboration inside FPGAs, the data buffering in the memory banks, the data communication between FPGAs and the external interface optical link (Figure 17).
Sixteen lines from the AD can generate up to 16 GByte/s of raw data at maximum sampling frequencies. JESD I/F IP core manages the physical interface and is connected with an internal bus to the data analysis core.
The effective board layout is horizontally mirrored, as shown in figure below, due to the JESD I/F GTX transceiver position in the FPGA package and the high speed layout requirements.

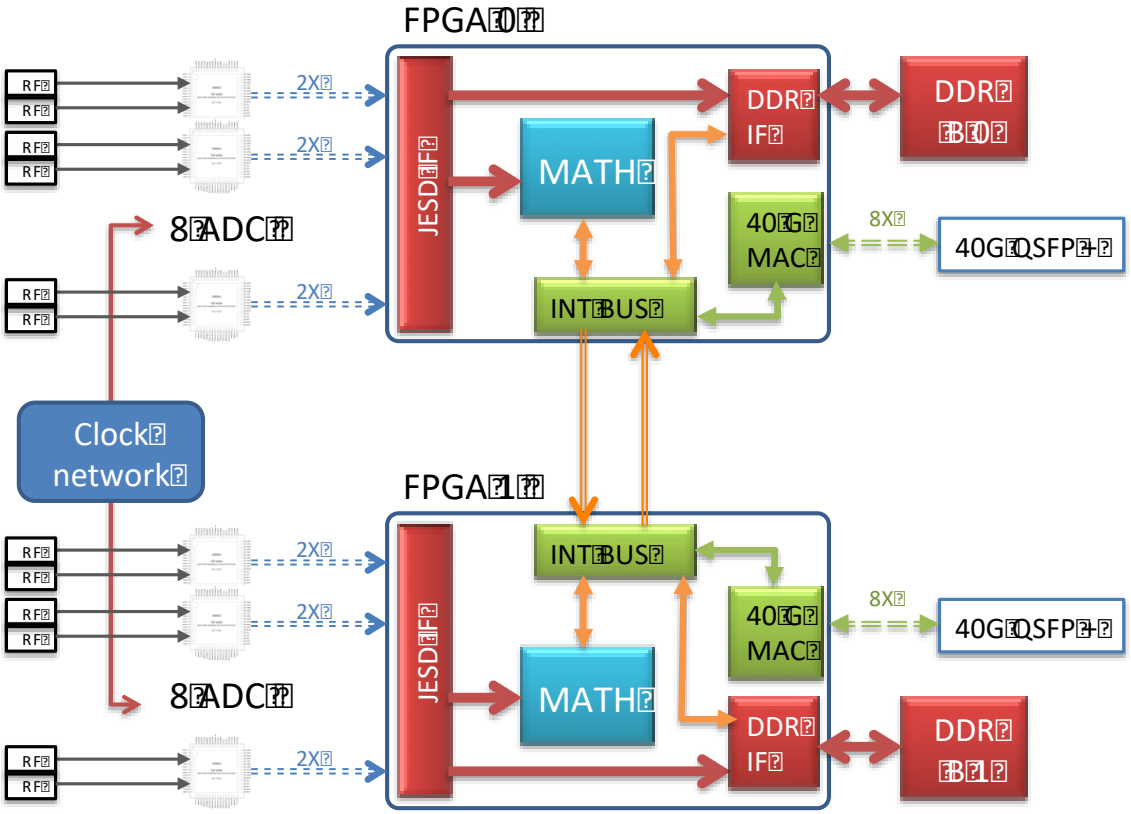


Figure 17. iTPM high speed data paths

The DDR 64 bit memory interface can perform up to 16GByte read or write operations (800 MHz clock) and can be connected to JESD interface to implement a 128M sample raw buffer.

The iTPM FPGAs are two identical devices that provide suitable and efficient resources to implement the main board data management and elaboration features.
Each FPGA provides the following interfaces:

- Management SELECT MAP for configuration, reconfiguration, monitoring and scrubbing
- Management bus interface to communicate with the management CPLD
- Management system monitor, check up to sixteen supply voltages from each FPGA and integrate voltage monitoring implemented by the U4 MCU device
- Sixteen JESD RX data links to receive data from the ADCs
- JESD clock inputs, one for the transceiver and one for the internal logic

- Four Multi-Gigabit (10G Ethernet or above) bidirectional data links connected to a QSFP+ connector to implement either 4x10G Ethernet interfaces or one 40Gbit Ethernet. The device line speed is higher than the Ethernet one: other communication standard can be evaluated.
- 10G Eth clock PLL input
- PPS input signal
- 64 bit DDR4 memory interface, 8 chip x8 on board soldered devices for each FPGA, up to 16 Gbit each (default 4 Gbit)
- 100 MHz DDR clock
- 6 high speed (12.5 Gbit each) differential lines FPGA to FPGA bus for a 60 Gbit full duplex bus (FPGA INTBUS).

The pinout of the two FPGA are identical with exception of the identity pin (A14, pull UP on FPGA0, GND on FPGA1) and the F2F transceiver functional allocation.
The two FPGAs can share the same configuration firmware. Due to layout restriction the corresponding transceiver on the two FPGA shall execute different functions. Application firmware shall manage that with internal data path switch.

7.5 Board synchronization and reset

iTPM board has two separated clock structures: the management clock tree and the acquisition clock tree.

7.5.1 Management clock tree

The management clock tree is sourced at 125 MHz by the Ethernet Phy to the CPLD. The CPLD generates the clock for the MCU and the local bus clock to the two FPGAs.
Each FPGA generates a data clock for the high speed RGMII-like data bus to the CPLD.

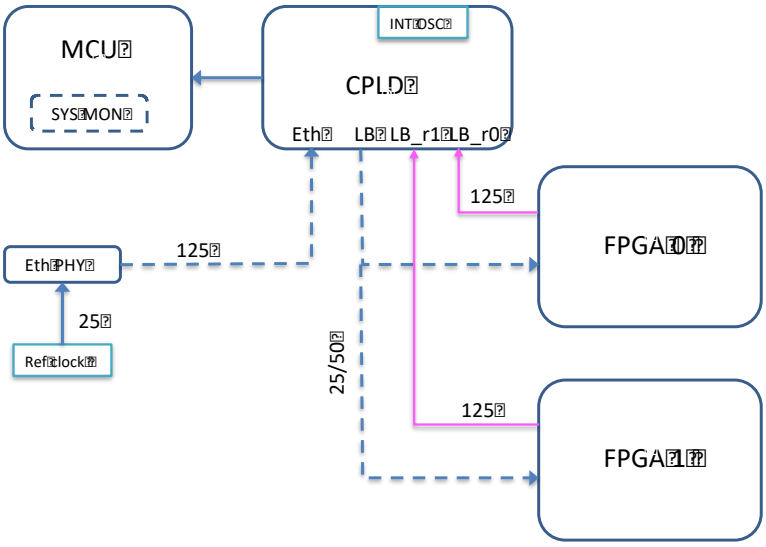


Figure 18. Management clock tree

The management CPLD generates reset and enable signals for all board active devices.

7.5.2 Acquisition clock tree

The board is organized in two symmetrical sides, one for each FPGA, with a common PLL to generate sampling and synchronization signal and another PLL for the Optical output link. A clock distribution network is provided for the sixteen AD to implement the JESD204B subclass 1 to guarantee the channel to channel synchronization.

Sampling clock network details are in the figure below. Sampling PLL (U40) can be sourced by a 10MHz on board oscillator (REF B) or by an external high quality 10MHz clock (REF A) to guarantee a fixed phase related acquisition and better clock noise performances. The U40 PLL implements the JESD204B with a synchronization input interface to receive the acquisition start signal and to generate a deterministic and clock synchronous start signal that is distributed with the same structure and devices as the clock signal. Clock and synchronization are generated directly by the PLL for each side of the board and four x8 clock buffer distribute the signals to all the devices. For each device a same length clock and SYSREF signal is provided by the board layout

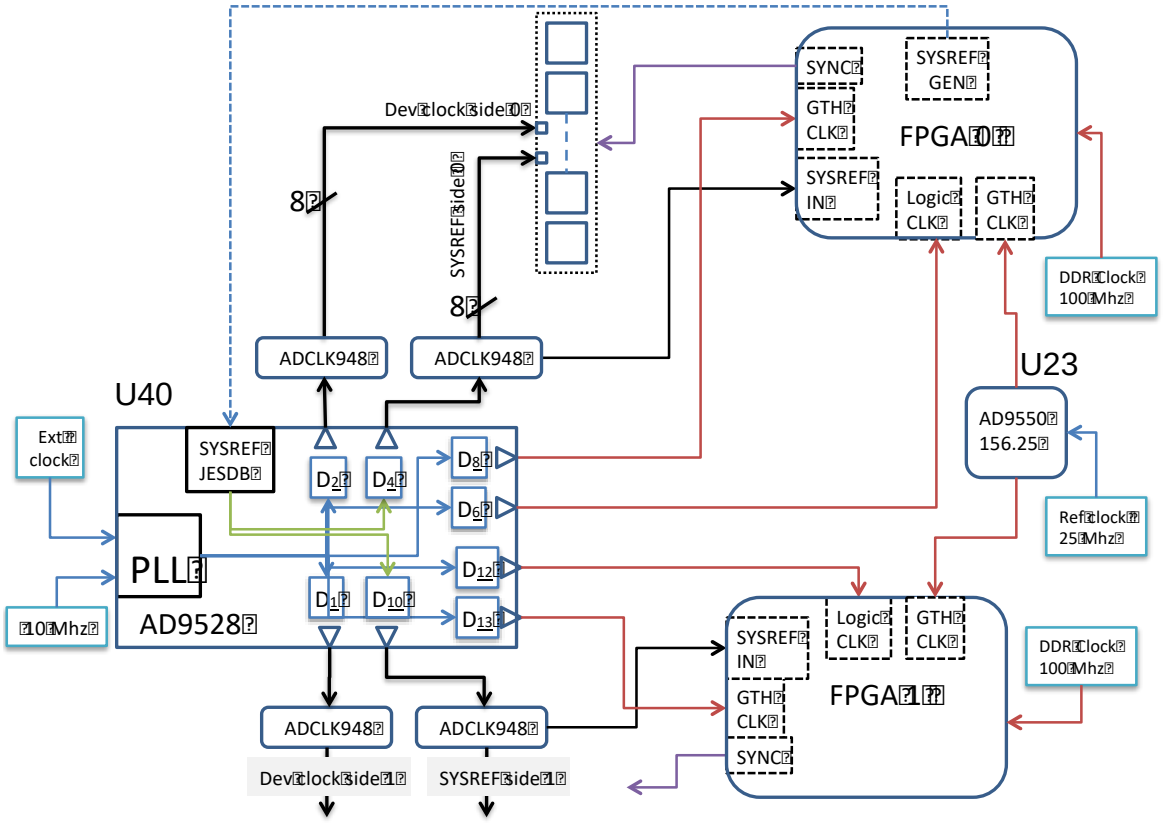


Figure 19. iTPM data clock network

PLL generates also a reference clock to the FPGA transceiver interface, GTH CLK, and a clock for the internal logic.
All the PLL outputs can be programmed to generate n/m divided frequency of the internal one.

All the unused output ports should be disabled to save power. Also the SYSREF distribution network can be disabled after the start of acquisition, to save power.

Specific PLL is provided to generate the clock required by the optical link (U23) and two 100 MHz clock generators, one for each FPGA, are provided to generate DDR clock.
FPGA internal structure provides wide capabilities to generate the data related clock frequencies starting from the provided external frequencies.
Further details on the system level synchronization feature can be found in Figure 20 and Figure 21. An external start signal, PPS, is received on the SMA connector (J14) and shared to both FPGAs via and opto-isolator. FPGA 0 shall generate the SYSREF signal to the PLL to enable the acquisition start for all the AD of the board. The same pins on the FPGA 1 are terminated to ground with 1KOhm resistors.
A return path of SYSREF from PLL to FPGAs is also available for generic purpose or to provide an extra clock source (not shown in Figure 19, Figure 20.).

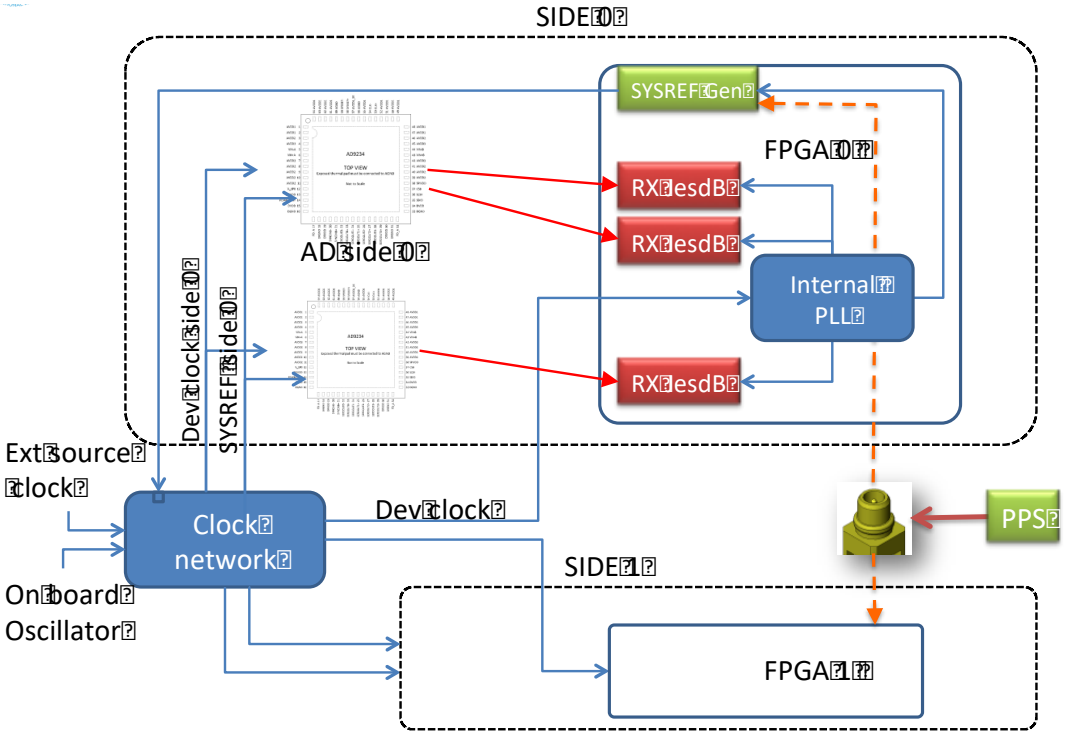


Figure 20. iTPM JESD SYSREF and PPS synchronization scheme

PLL configuration starts from the external 10 MHz input frequency and the precise 100 MHz VCXO available on the board.
The PLL reference A is sourced from the backplane interface, coming from the Subrack management PLL.
Alternatively the PLL reference B can be selected and it is sourced from the J1 connector available on the board.

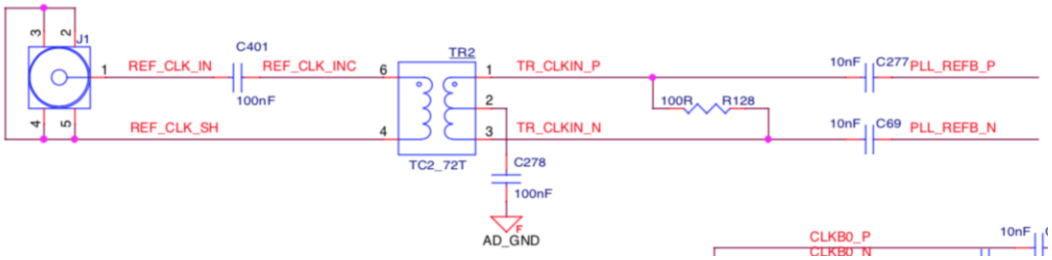


Figure 21. 10 PLL ref B MHz reference clock input circuit

PLL switch-over circuit shall be programmed with PLL SPI interface available from management CPLD (see AD9528 datasheet).

Sampling clock shall be programmed to output 1 and 2 with LVDS 3,5 mA mode divided sampling clock shall be programmed for FPGA MGT, to be used as reference and to the internal user logic, to be used as internal data path related clock.

SYSREF signal propagation network is almost the same of the clock one but due to the non-periodic function (SKA configuration requires only a start signal for each continuous acquisition session) HSTL output shall be configured due to different signal terminations.
SYSREF PLL output and corresponding clock buffer (U43, U44), can be powered off during continuous acquisition to save about 2W of power.
The SYSREF return signal to both FPGAs shall be turned off, if unused.

8. BOARD EXTERNAL INTERFACES

In this chapter the iTMP board external interfaces are introduced.

8.1 LEDs

Eight LEDs are available on board, as listed below.

Reference	Signal	Op. status	Description
LD2	MAN_DONE	“ON”	U1, CPLD configuration DONE status, High = “ON”
LD3	MAN_PG	“OFF”	U61 (i.e. TPS54418), U62, U63 (i.e. ADP1741) wired and Power good in, High= “OFF”
LD4, LD5	XO2_USR_LED0,1	-	User status indicator, High = “ON”
LD1, LD6	MCU_USR_LED0,1	“OFF”	MCU user selectable
LD7	XIL0_DONE	“ON”	U2, FPGA 0 configuration DONE status, High = “ON”
LD8	XIL1_DONE	“ON”	U3, FPGA 1 configuration DONE status, High = “ON”

Table 16 LEDs

LD3 is a wired AND of the power good of the management DC-DC converter. If this led is ON a management DC supply issue is present, the board shall be shut-down and verified.

8.2 Connectors and Jumpers

Reference	Part number	Description
J1	MMCX-J-P-H-ST-MT1	mSMA, Reference clock input
J2, J3	FQSFP_HS	FLY OVER high speed QSFP+, 40G interface
J11, J12	FQSFP_LS	FLY OVER low speed and supply
J4	QFS016-D-RA	Backplane signal connector
J7	HEADER_2x4	CPLD JTAG
J8	HEADER_2x4	XIL_JTAG
J9	HEADER_1x4	CPLD UART
J10	HEADER_1x4	MCU UART0
J13	HEADER_2x4	MCU UART1 & reset
J15,J16,J17,J18	IP5-08-05.0-L-S-1-L-TR (1)	RF IN CONNECTOR
J20,J21	ERF8-010-05.0-L-DV-TR	EXPANSION INTERFACE
J22	UPT-04-01-01-L-RA-LC-TR	Backplane POWER IN
J25	HEADER_1x4	FPGA0 GPIO
J26	HEADER_1x4	FPGA1 GPIO

Table 17. Connectors

(1) IJ5-08-05.0-L-S-1-TR alternative is available upon request (TBV)

8.3 JTAG and UART debug interfaces

Separate JTAG and debug interfaces are available for the iTPM devices: CPLD JTAG, FPGA JTAG and MCU UARTs. The two Xilinx FPGA JTAG are accessible through the management CPLD by the external J8 standard Xilinx JTAG connector, supplied at 3,3V or directly from the management CPLD that can implement a JTAG bridge vs the internal register bus.
The board is provided with a standard CPLD firmware that implements the routing of the Xilinx JTAG bus in the standard daisy chain from the external connector to the FPGA0 and FPGA1.
The J8 external interface has been buffered to allow a 3,3V supply on the external cable side and the 1,8V supply on the internal FPGA bank supply operating at maximum speed.

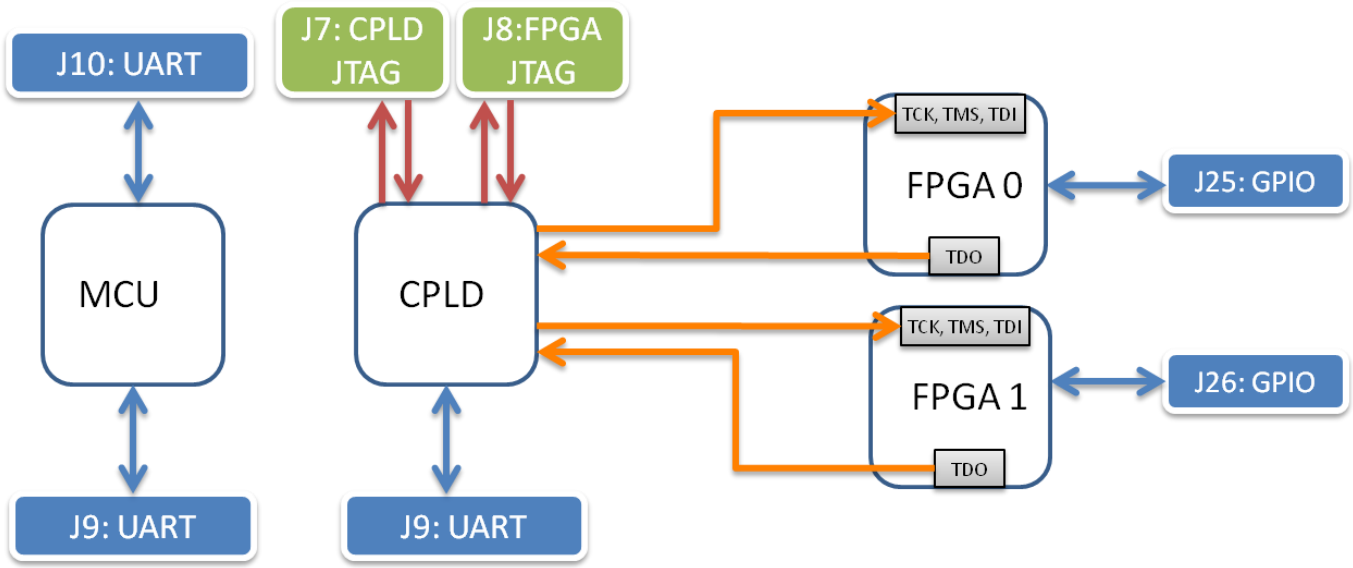


Figure 22. iTPM internal debug interface

The virtual cable firmware option is an usefull enhancement: it has been planned as for future CPLD versions to virtualize the external physical cable and operate remote standard JTAG debug operation directly on the existing gigabit ethernet management link.
CPLD internal JTAG routing can be configured setting the suitable register *regfile_jtag_sel*, address 0x30000008 with one of the following scheme: (options 4-6 TBD):

regfile_jtag_sel	**JTAG INTERFACE**	**Board JTAG Connection scheme**
0x00, 0x11 (default)	External, J8	FPGA0 => FPGA1
0x01	External, J8	FPGA0
0x10	External, J8	FPGA1
n.a.	Internal, ethernet virtual cable	FPGA0=> FPGA1
n.a.	Internal, ethernet virtual cable	FPGA0
n.a.	Internal, ethernet virtual cable	FPGA1

8.3.1 MCU Debug and UART/GPIO

MCU debug connector J10, J11 integrates the programming interface and a UART/GPIO interface.

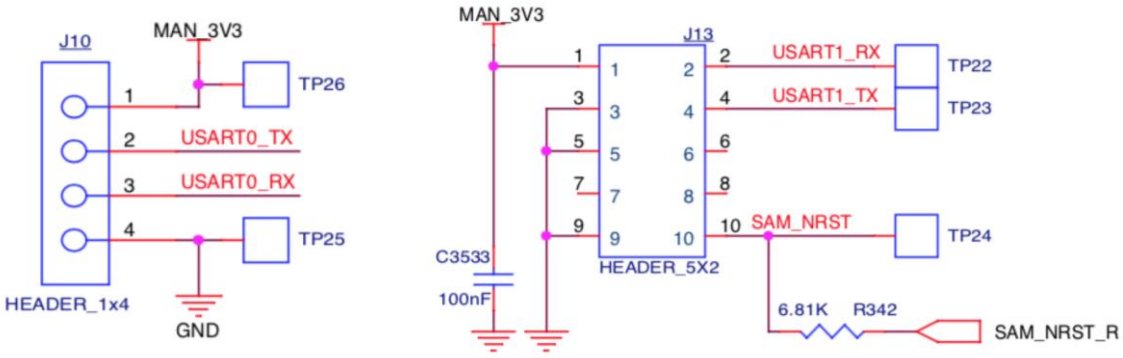


Figure 23. J10, J11 schematic

8.3.2 CPLD JTAG Connector

CPLD JTAG J7 is wired with a double row 2.54 mm through hole connector.

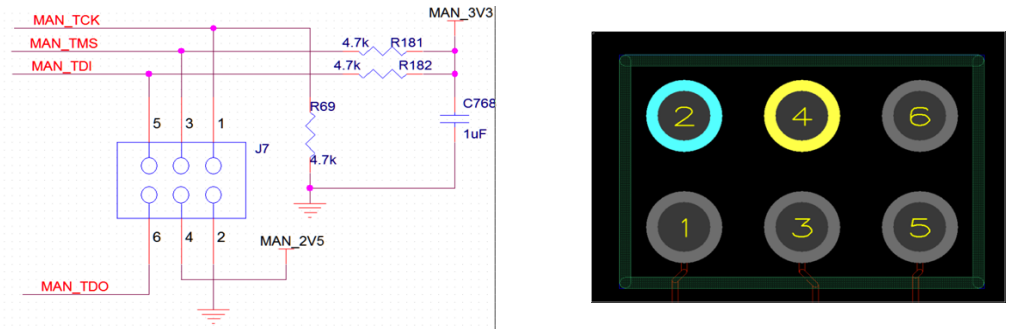


Figure 24. U1 J7 JTAG schematics and footprint

8.3.3 CPLD UART Connector

CPLD UART:

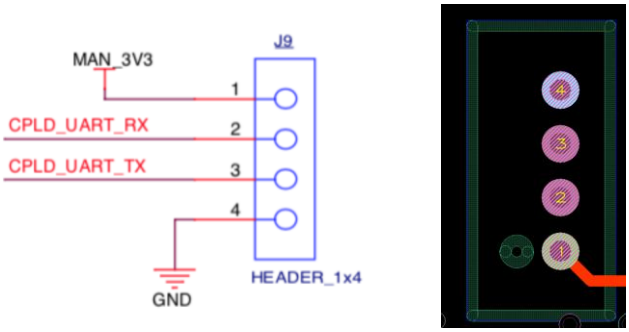


Figure 25. U1 J9 UART schematics and footprint

8.3.4 FPGA JTAG Connector

FPGA JTAG, is connected as specified in the Figure 22. The external reference supply can be selected to 3,3V (default) or to 1,8V to bypass the internal buffers.

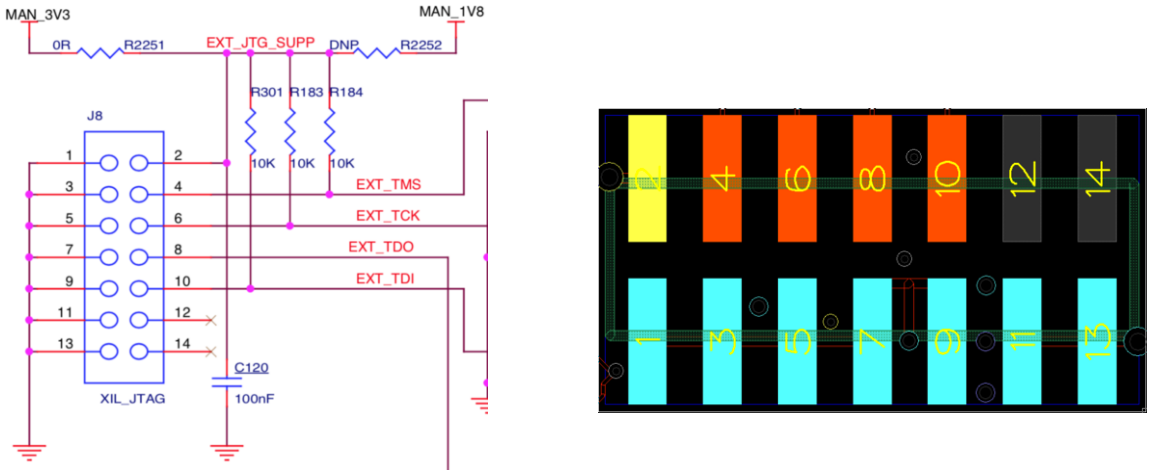


Figure 26. FPGA J6 JTAG connector and footprint

8.4 Ethernet I/F 40 Gbit

Each FPGA is connected with four 10G links to a QSFP+ FLY-Over interface to implement one 4x10G Ethernet interface or one 40G Ethernet interface.
The adopted FLY-Over interface allows to place the QSFP cage on a separated board connected with high speed differential cable for main data and low speed cable for supply and low speed management IO.
FPGA0 is connected to J2, FPGA1 to J3 connector with the High speed FQSF transceiver signals with DC connection (FPGA pinout in [RD2]); all the required line terminations are inside FPGA devices and QSFP+ module.
Two separate dedicated low speed I2C interfaces (10GE0,1 I2C) are connected to management CPLD to interface the remote QSFP and I/O expander I2C interface [RD9].
QSFP+ connectors are supplied with MAN_3V3 source, always active.

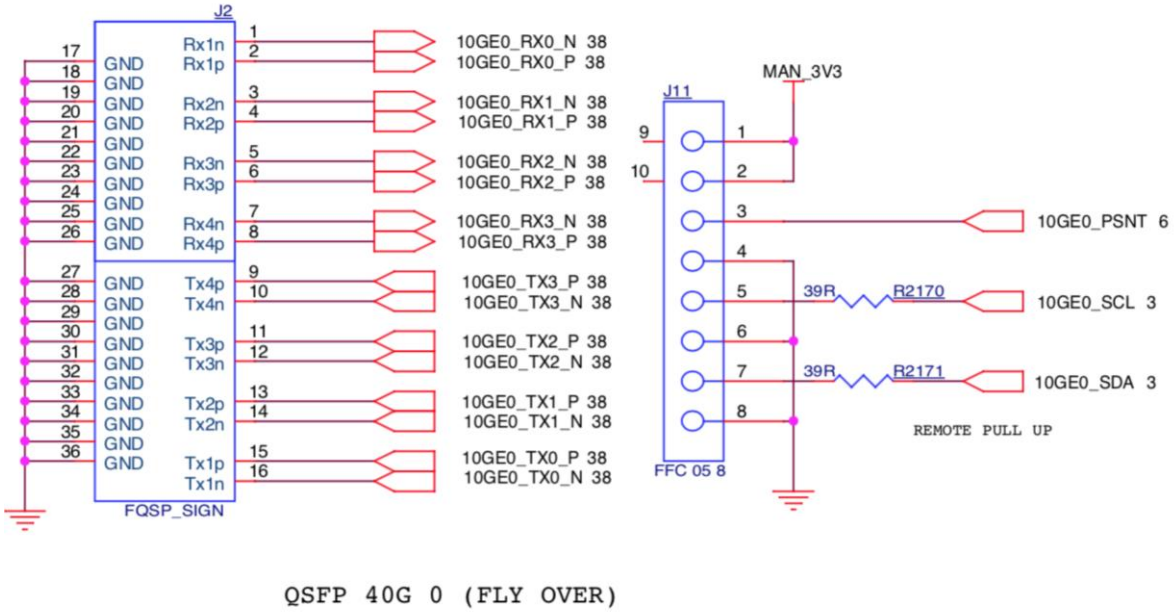


Figure 27. QSFP Fly Over Interface J2, J11 schematics

8.5 iTPM AD acquisition interface

iTPM board has 32 analog inputs distributed on 4 high density RF connectors placed on one side of the board. Each channel provides the same front end circuit that is connected to the Analog to Digital converter.
The front-end has been designed with RF active interface (Figure 28) or passive interface (Figure 29). The choice is done at board production step with different part list on the same circuit board; the difference is the component from the RF connector to the AD converter, while data processing and acquisition structure are the same. Additionally, the total board power need is quite different and the amplifier supply is not needed in the passive configuration.
Input signals are expected 50 Ohm single end; both circuits have been evaluated to work in the range 35 Mhz-1000 Mhz.

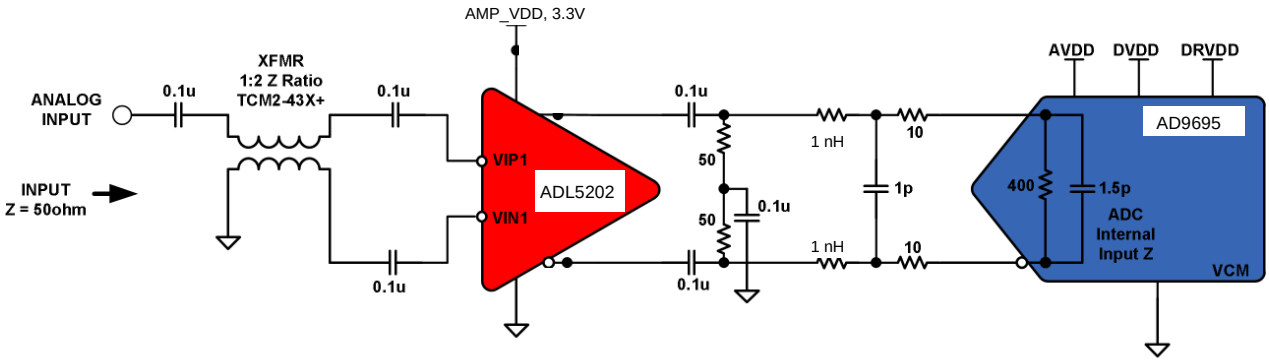


Figure 28. RF Active front end design

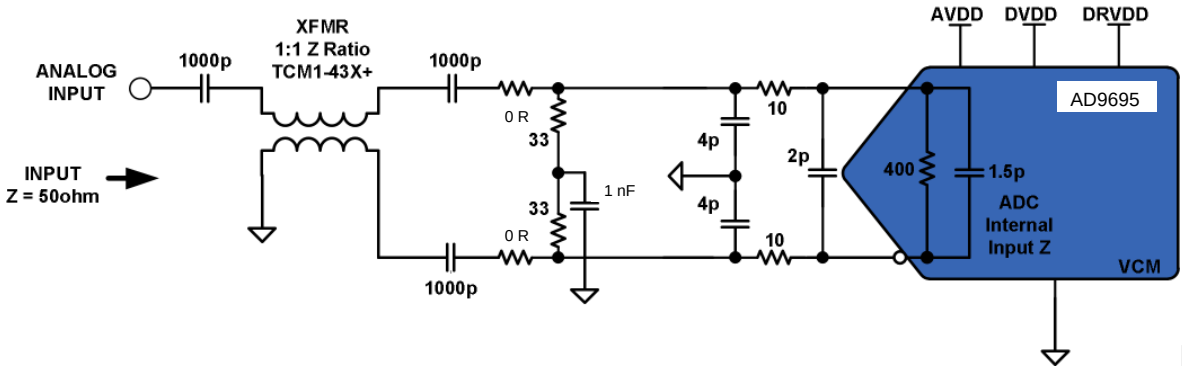


Figure 29. RF Passive front end design

ADL5205 and AD9695 control interfaces are detailed in “Analog interface configuration” section, chapter 10.2. Both SPI and direct pin control are available through the management CPLD for dynamic configuration over all the 32 input channels.

The front-end configuration is done only in production. In each case, no stubs or floating traces are present in the board circuit.

Amplifier and Analog to digital converter shall be configured by the user to the proper value as shown in the corresponding figures.

8.6 Analog Front-End interface

iTPM can be connected with two identical RF fiber interface boards, one for each side of the circuit. These boards interface sixteen antennas RF fiber each providing mechanical interface and analog signal conditioning before the digital conversion. iTPM provides supply and digital control signals to these two boards through J20 and J21 connectors, placed symmetrically on the two sides of the board.
Each connector can provide 5,0V supply filtered from the internal global supply (currently not available, ferrite unpopulated) and a DC-DC dedicated supply, 3,5 V, nominal 2,5A, filtered with ferrites, to be enabled with the control signal (EN_FE0_3V5 for J20, EN_FE1_3V5 for J21, default disabled).
Digital control signals are connected with a series 39Ohm resistor to the management CPLD and are organized in a SPI bus, a reset signal and two generic control signals. Connections between connector and CPLD pin are listed in the table below.

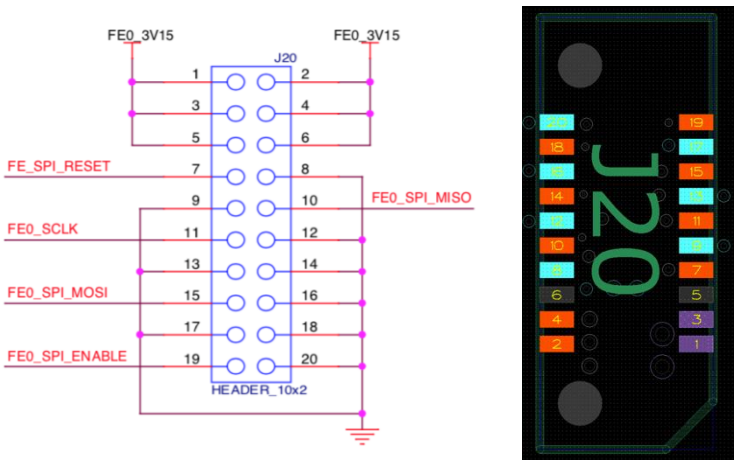


Figure 30. J20 schematics and connector physical footprint

Current outputs FE0_3v15 and FE1_3v15 are monitored with current and voltage measures.

CPLD Signal	iTPM signal	Default value	iTPM BUS	I/O Standard
MAN_FE0R_0	FE0_SPI_RESET		FE0_SPI	LVT330 S 4 mA
MAN_FE0R_1	FE0_SPI_MISO			LVT330 S 4 mA
MAN_FE0R_2	FE0_SCLK			LVT330 S 4 mA
MAN_FE0R_3	FE0_SPI_MOSI			LVT330 S 4 mA
MAN_FE0R_4	FE0_SPI_ENABLE			LVT330 S 4 mA
MAN_FE1R_0	FE1_SPI_RESET		FE1_SPI	LVT330 S 4 mA
MAN_FE1R_1	FE1_SPI_MISO			LVT330 S 4 mA
MAN_FE1R_2	FE1_SCLK			LVT330 S 4 mA
MAN_FE1R_3	FE1_SPI_MOSI			LVT330 S 4 mA
MAN_FE1R_4	FE1_SPI_ENABLE			LVT330 S 4 mA

Table 18. FE connection to management CPLD

9. BOARD INTERNAL INTERFACES

This chapter deals with the iTMP board internal interfaces.

9.1 AD JESD204B data interface

The sixteen analog to digital converter AD9695 digital data interfaces are connected to the Xilinx GTX receivers for the MultiGigabit links and to a GPIO bank for the required control signals.
Since only sixteen receivers for FPGA are available, only two data links of each AD are connected to provide an eight-bit interface.

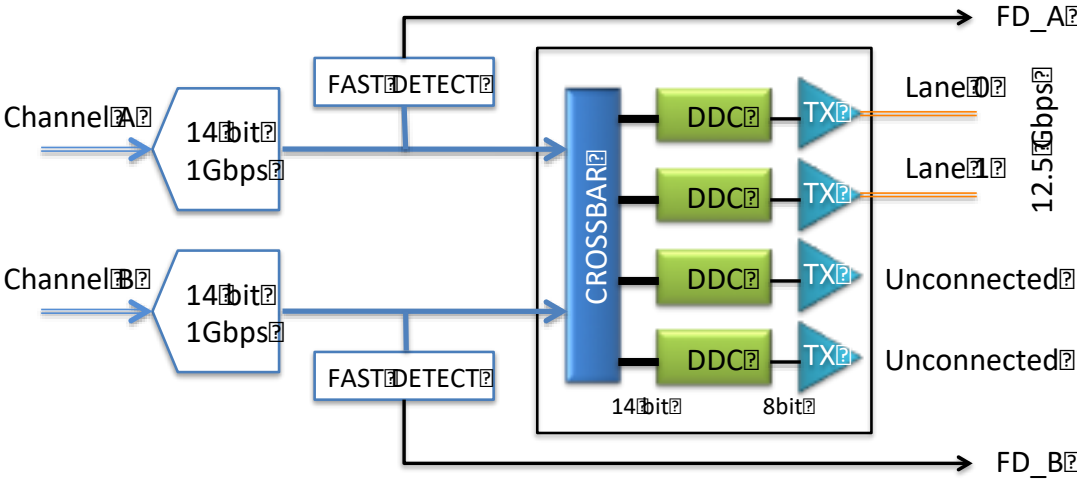


Figure 31. Analog to Digital JESDB data interface

High speed links 0,1 are connected from each AD to FPGA, link 2,3 are left unconnected. The outputs 0 of the AD n are named ADn_SERD0_P, ADn_SERD0_N and the outputs 1 of the AD n are named ADn_SERD1_P, ADn_SERD1_N

Fast detect outputs are CMOS output connected directly to the related FPGA, named And_FD_A, And_FD_b; these flags signals are related to each input channel to monitor the clipping of the incoming analog signal.

SyncB+ signal (not shown in figure) is connected from each ADC to the FPGA (named ADn_SYNC_P) with single-ended configuration to save power and reduce board connections; signal voltage conversions to the 2,5V FPGA banks are done with resistor dividers.

9.2 FPGA to FPGA Internal Bus

To complete iTPM capabilities a high speed bus that connects the two FPGAs is provided. This bus has been designed to have maximum speed and low digital noise. To meet this specification, six transceiver differential lines have been chosen.
The bus is organized over two FPGA MGT banks with 4+2 data lanes connected.
The bus is designed to operate with a configurable speed with a dedicated clock lines available for the bank PLL, independent from the one configured for the 40G Eth. Maximum line speed can reach 12.5Gbit/sec with the slowest Xilinx device speed grade (16.3 Gbit/sec with the fastest).

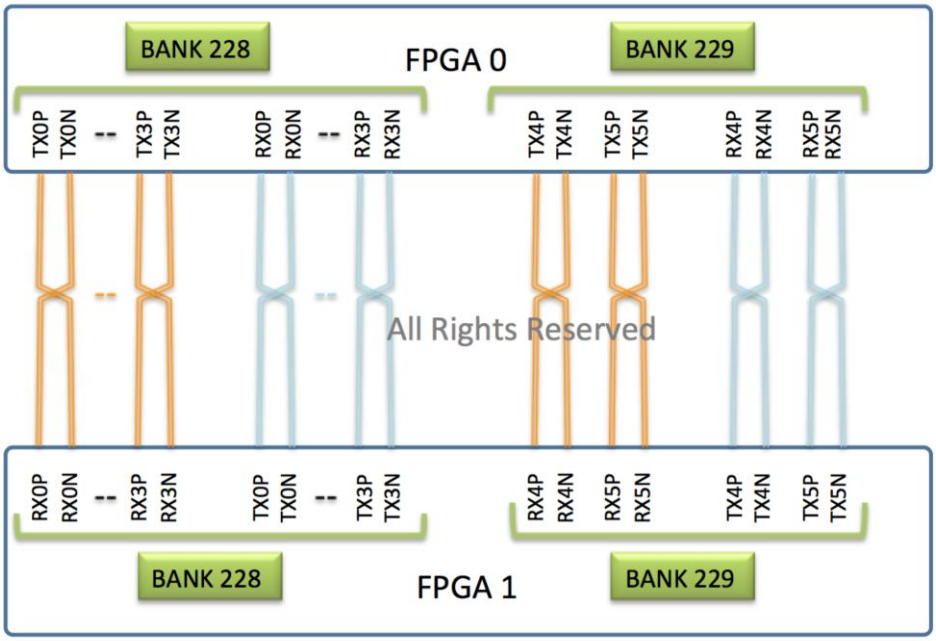


Figure 32. iTPM FPGA 2 FPGA internal bus

Due to layout constraints the connection scheme of the transceiver is not identical for the two FPGAs. The same number of lines are connected for each bank but the transceivers used are not the same. The application firmware shall manage that difference with the FPGA identity PIN and the required configuration steps.

9.3 FPGA to FPGA backplane Bus

Each of the two ADU 1.6 FPGAs implements a direct connection with the same position FPGAs of the previous and following position on the LFAA backplane with a single direction data line from the FPGA on the ADU placed on the first backplane slot to the ones on the last slot. This connection is implemented with a transceiver couple hosted on the same FPGA banks involved for the internal FPGA2FPGA bus.
Signal names, referenced in the [RD2] are:

- FPGA0, bank 229, FPGA0_EXTBUS_TX_P/N, FPGA0_EXTBUS_RX_P/N;
- FPGA1, bank 228, FPGA1_EXTBUS_TX_P/N, FPGA1_EXTBUS_RX_P/N.

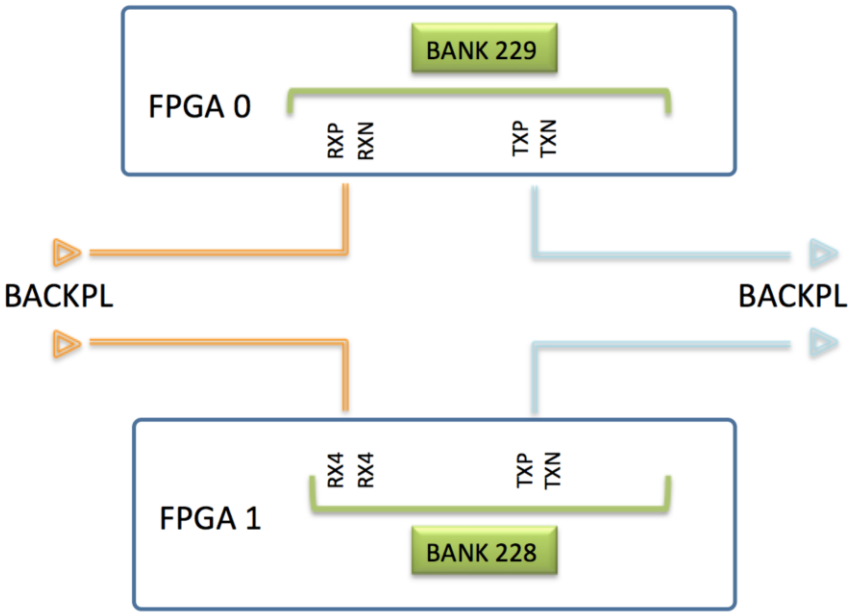


Figure 33 direct ADU to ADU connection scheme

NOTE: On the LFAA backplane rev 1.1 both the physical connections are available only on the internal TPMs, while the first and the last TPM have only one side connected, and the other side is terminated to a 100 ohm resistor [RD10]. This capability is not implemented on the backplane rev1.0.

9.4 DDR4 Interface

Each FPGA provides a 8-byte wide DDR interface connected with the FLY-BY topology. Eight 8 bit wide, 256M depth (4 Gbit devices) can accept for read or write operation the raw data coming from AD interface limited by memory depth.
Address bus can support 1G address space (16 Gbit devices), TBV.

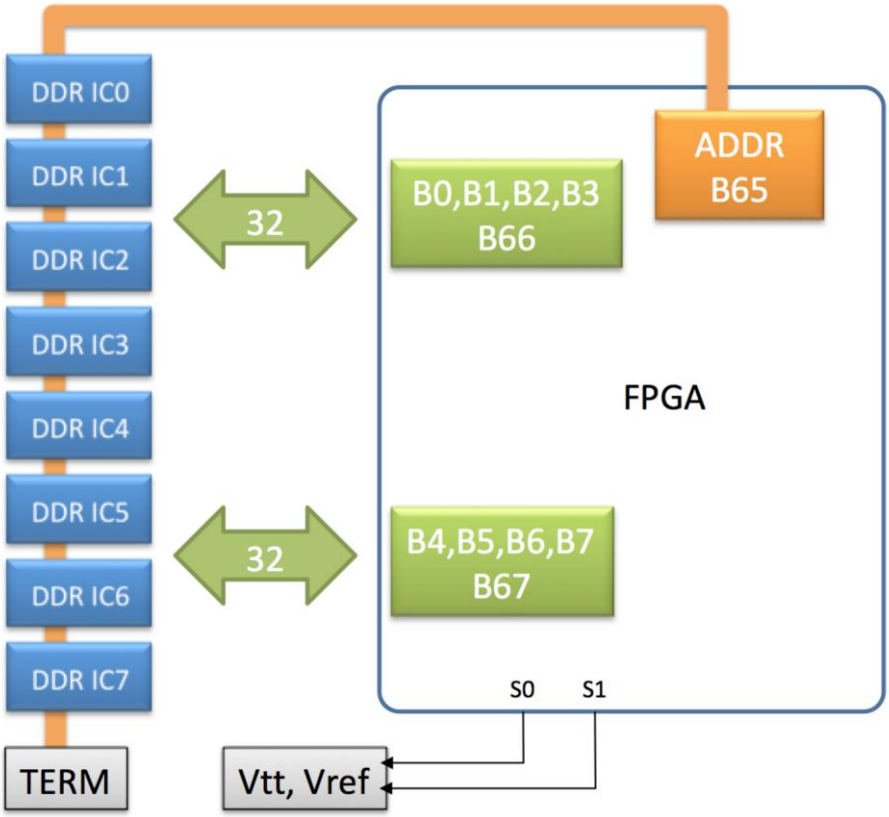


Figure 34. DDR interface topology

Address, command, clock and control lines are connected sequentially to all memory devices and are terminated at line end.

All DDR devices and FPGA I/O voltages are supplied by DDR_VDD (common for both FPGAs) that shall be enabled by the management.

Termination and Vref supply are separated for each FPGA and dynamic control signal shall be generated directly by the memory interface controller.

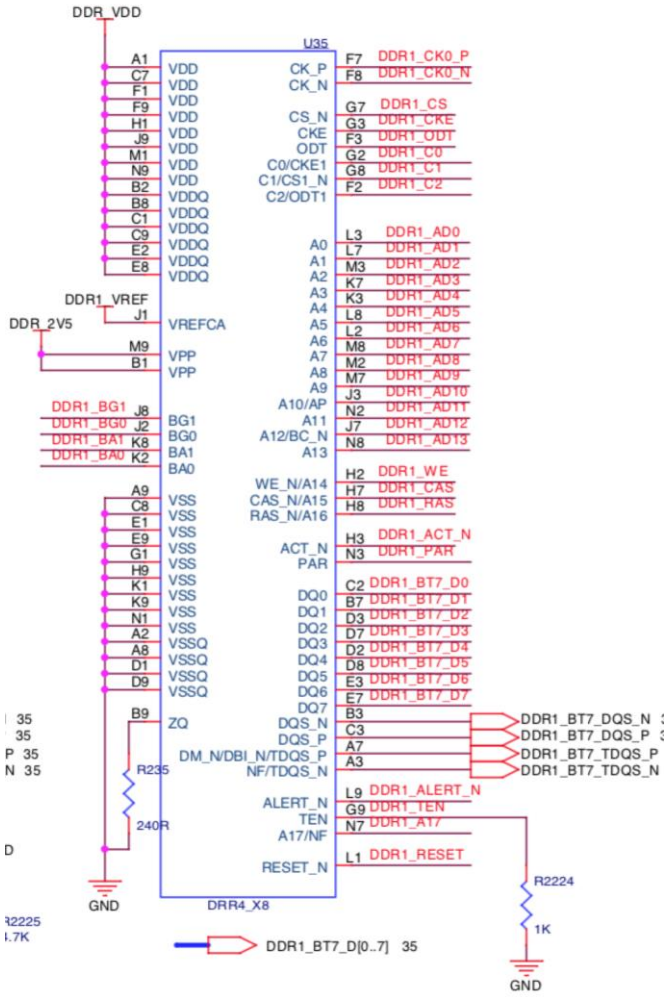


Figure 35. DDR memory connections

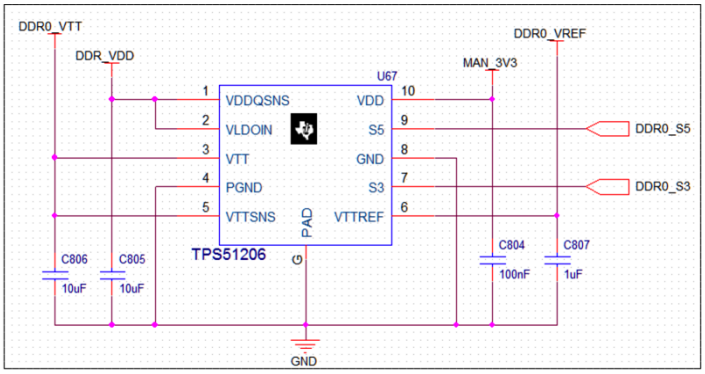


Figure 36. DDR Vtt and Vref supply



Figure 37. DDR ADDR & CMD terminations

10. BOARD CONFIGURATIONS

10.1 I/O buffer configurations

FPGA I/O buffers and CPLD I/O buffers shall be configured according to the connected trace characteristic.
High speed buses are impedance-matched and correct driver standard and impedance shall be configured; in specific situations also driver strength option is available to change the signal rise/fall time.
Faster options require more absorbed power: in the following table suggested configuration and bus speed are reported. These results are in accordance with post layout Signal Integrity simulations executed with I/O IBIS model and realistic data patterns (PRBS 7).

iTPM BUS	Device; line type	I/O standard	Buffer	Max speed
LOCAL BUS	U1, Bank1, 1.8V <-> U2, U3; Bank 49,1.8V bidirectional			
	MAN_LB_xx,, 100 Mbps	LVCMOS 1.8	Slow, 8 mA	100 Mbps
	MAN_LB_xx, 50 Mbps	LVCMOS 1.8	Slow, 4 mA	50 Mbps
	U2,U3 Bank 64 -> U1, Bank2, 3.3V, monodirectional			
	U1, RGMII IN , 100 Mbps	LVDS IN		250 Mbps
	U2, U3, RGMII OUT	LVDS OUT	TBD, 8 mA	250 Mbps
FSPI BUS	U1, 1,8V	LVCMOS 1.8	Normal, 4 mA	125 Mbps
DDR IF	U2, U3; 1.2V			
	Apply Xilinx MIG I/O specification			
SPI 0 (FLASH)	U1, 3.3V			
	SDIO, SDCK, 100 Mbps	LVTTL	Slow, 8 mA	100 Mbps
	SDEN	LVCMOS 3.3	Slow, 4 mA	25 MHz
SPI 1 (VGA)	U1, 3.3V			
	SDIO, SDCK, 100 Mbps	LVCMOS 3.3	Slow, 8 mA	100 Mbps
	SDIO, SDCK, 50 Mbps	LVCMOS 3.3	Slow, 4 mA	50 Mbps
	SDEN	LVCMOS 3.3	Slow, 4 mA	25 MHz
SPI 2 (AD)	U1, 1.8V			
	SDIO, SDCK, 100 Mbps	LVCMOS 1.8	Slow, 8 mA	100 Mbps
	SDIO, SDCK, 50 Mbps	LVCMOS 1.8	Slow, 4 mA	50 Mbps
	SDEN	LVCMOS 1.8	Slow, 4 mA	25 MHz
SPI 3 (PLL)	U1, 3.3V			
	All, 100 Mbps	LVCMOS 3.3	Slow, 4 mA	100 Mbps
SPI FE (J20,J21)	U1, 3.3	LVTTL	Slow, 4 mA	TBD

Table 19. IO buffer configurations

Xilinx controlled impedance DCI feature, if enabled, absorbs static power; drive and receive DCI capability shall be activated selectively in accordance with selected functionality.
Xilinx GTX multi gigabit transceiver optimal configuration shall be defined with functional analysis with the Xilinx tool in the field conditions.

10.2 Analog interface configuration

Analog devices are configured by three separate SPI buses and some control signals. The configuration and monitoring process is executed through the Management CPLD: the main FPGAs are not involved in these operations.

10.2.1 Analog amplifiers interface, SPI 1

The 32 analog amplifiers (ADA) are connected by the SPI 1 bus and some static control signals. To obtain a single device access capability and to maintain the fan-out of all the signals under eight, the following connection matrix has been adopted between CPLD and the devices:

ADA devices connection matrix	**ADA_SDIO0**	**ADA_SDIO1**	**ADA_SDIO2**	**ADA_SDIO3**
	ADA_SDCK0	**ADA_SDCK1**	**ADA_SDCK2**	**ADA_SDCK3**
ADA_SDEN0	ADA0	ADA8	ADA16	ADA24
ADA_SDEN1	ADA1	ADA9	ADA17	ADA25
ADA_SDEN2	ADA2	ADA10	ADA18	ADA26
ADA_SDEN3	ADA3	ADA11	ADA19	ADA27
ADA_SDEN4	ADA4	ADA12	ADA20	ADA28
ADA_SDEN5	ADA5	ADA13	ADA21	ADA29
ADA_SDEN6	ADA6	ADA14	ADA22	ADA30
ADA_SDEN7	ADA7	ADA15	ADA23	ADA31

Table 20. ADA devices connection matrix

CPLD SPI interface signals Enable, Data and clock shall be gated to access to the desired device.
Line series terminations are provided to avoid large signal reflection; CPLD buffer shall be configured with “LVT330 S mA” and maximum bus speed is 25MHz.

Some ADA pins are available for direct configuration. These signals are connected all together and shall be controlled with a configuration register.

iTPM signal	**U1 Pin**	**iTPM BUS**	**Default value**	**I/O Standard**
ADA_A0_R	E13	ADA_CTRL	LOW	LVT330 S 8 mA
ADA_A1_R	A6	ADA_CTRL	LOW	LVT330 S 8 mA
ADA_FA_R	B5	ADA_CTRL	LOW	LVT330 S 8 mA
ADA_LATCH_R	B6	ADA_CTRL	LOW	LVT330 S 8 mA
ADA_LP_R	A5	ADA_CTRL	LOW	LVT330 S 8 mA
ADA_MODE_R	E6	ADA_CTRL	HIGH	LVT330 S 8 mA
ADA_PWUP	B9	ADA_CTRL	HIGH	LVT330 S 8 mA

Table 21. ADA device configuration signals

Due to the large fan-out these signals of the CPLD shall be configured with 8mA of output current driver. These signal are considered almost static and the required value shall be configured at least 100ns before normal operations.

10.2.2 Analog to digital converters, SPI 2

The sixteen analog to digital converters are connected to the SPI 2 bus and to the “powerdown” signal. The connection matrix between the CPLD and the AD, with the same approach like VGA, is the following:

Analog to digital converters connection matrix	**AD_SDIO0**	**AD_SDIO1**	**AD_SDIO2**	**AD_SDIO3**
	AD_SDCK0	**AD_SDCK1**	**AD_SDCK2**	**AD_SDCK3**
AD_SDEN0	AD 0	AD 4	AD 8	AD 12
AD_SDEN1	AD 1	AD 5	AD 9	AD 13
AD_SDEN2	AD 2	AD 6	AD 10	AD 14
AD_SDEN3	AD 3	AD 7	AD 11	AD 15

Table 22. Analog to digital converters connection matrix

Line series terminations are provided to avoid large signal reflection; CPLD buffer shall be configured with “LVT180 S 4 mA” and maximum bus speed is 25MHz.
The “powerdown” control signal has a large fan-out so shall be configured with “LVT180 S 8mA”

10.2.3 Sampling PLL interface, SPI 3

The PLL that generates the analog to digital sampling clock and the JESD synchronization architecture is configured with the SPI3 bus and some control signals from CPLD.

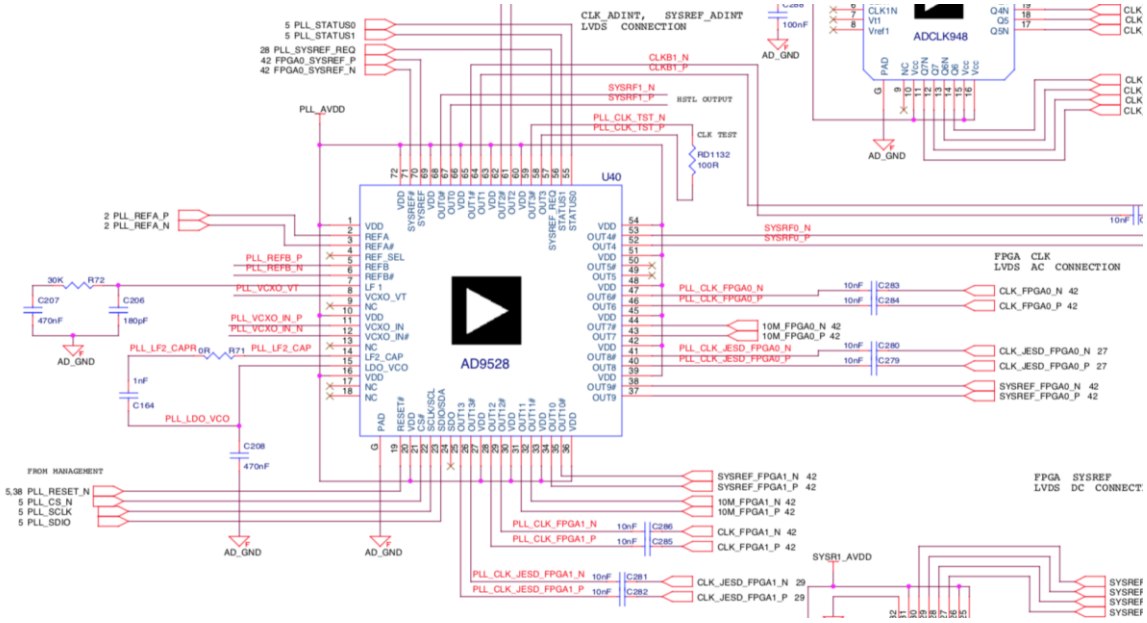


Figure 38. iTPM sampling PLL, detail

Configuration signals are directly connected with CPLD; line series terminations are provided to SPI clock and data lines to minimize signal noise during SPI access operations.

iTPM signal	U1 Pin	iTPM BUS	Default value	I/O Standard
PLL_CS_N	T12	PLL_CTRL	LOW	LVT330 S 4 mA
PLL_RESET_N	M9	PLL_CTRL	HIGH	LVT330 S 4 mA
PLL_SCLK_R	P12	SPI 3	LOW	LVT330 S 4 mA
PLL_SDIO_R	T13	SPI 3	HIGH Z	LVT330 S 4 mA
PLL_STATUS0	N10	PLL_CTRL	INPUT	LVT330 S 4 mA
PLL_STATUS1	R11	PLL_CTRL	INPUT	LVT330 S 4 mA

Table 23. PLL connections

11. BOARD START-UP

At power up the management components (CPLD, MCU) of the iTPM board start up with the provided BIOS version; the FPGAs and the acquisition circuit is power down, unless a specific BIOS flag requires the FPGA device power up and the FPGA bitstream programming from FLASH memory .
When the ethernet management functions are available, the user shall access the CPLD registers and enable the other devices, through a minimal set of SW functions (API interface).

12. CONNECTION TABLES

12.1 PLL

Pin Name	Pin	iTPM signal	Electrical standard	Function
CS#	21	PLL_CS_N	CMOS 3,3	Chip select, from U1
OUT0	67	SYSRF1_P	HSTL	SYSREF to AD 8-15
OUT0#	68	SYSRF1_N	HSTL	
OUT1	64	CLKB1_P	LVDS	Sampling CLOCK to AD 8-15
OUT1#	65	CLKB1_N	LVDS	
OUT2	61	CLKB0_P	LVDS	Sampling CLOCK to AD 0-7
OUT2#	62	CLKB0_N	LVDS	
OUT3	58	PLL_CLK_TST_P	LVDS	Clock test point
OUT3#	59	PLL_CLK_TST_N	LVDS	
OUT4	52	SYSRF0_P	HSTL	SYSREF to AD 0-7
OUT4#	53	SYSRF0_N	HSTL	
OUT5	49	nc	-	-
OUT5#	50	nc	-	-
OUT6	46	PLL_CLK_FPGA0_P	LVDS	User logic clock, FPGA 0
OUT6#	47	PLL_CLK_FPGA0_N	LVDS	
OUT7	43	nc	-	-
OUT7#	44	nc	-	-
OUT8	40	PLL_CLK_JESD_FPGA0_P	LVDS	MGT ref clock for JESD link, FPGA 0
OUT8#	41	PLL_CLK_JESD_FPGA0_N	LVDS	
OUT9	37	SYSREF_FPGA0_P	LVDS	Optional SYSREF to FPGA 0
OUT9#	38	SYSREF_FPGA0_N	LVDS	
OUT10	34	SYSREF_FPGA1_P	LVDS	Optional SYSREF to FPGA 1
OUT10#	35	SYSREF_FPGA1_N	LVDS	
OUT11	31	nc	-	-
OUT11#	32	nc	-	-
OUT12	28	PLL_CLK_FPGA1_P	LVDS	User logic clock, FPGA 1
OUT12#	29	PLL_CLK_FPGA1_N	LVDS	
OUT13	25	PLL_CLK_JESD_FPGA1_P	LVDS	MGT ref clock for JESD link, FPGA 1
OUT13#	26	PLL_CLK_JESD_FPGA1_N	LVDS	
REF_SEL	4	-	-	-
REFA	2	PLL_REFA_P	LVDS/HSTL	Backplane 10 MHz clock reference
REFA#	3	PLL_REFA_N	LVDS/HSTL	
REFB	5	PLL_REFB_P	LVDS/HSTL	External 10 MHz clock reference
REFB#	6	PLL_REFB_N	LVDS/HSTL	
RESET#	19	PLL_RESET_N	CMOS 3,3	Reset from U1
SCLK/SCL	22	PLL_SCLK	CMOS 3,3	SPI 3
SDIO/SDA	23	PLL_SDIO	CMOS 3,3	SPI 3
SDO	24	nc	-	-
STATUS0	55	PLL_STATUS0	CMOS 3,3	PLL status 0, to U1
STATUS1	56	PLL_STATUS1	CMOS 3,3	PLL status 1, to U2
SYSREF	70	FPGA0_SYSREF_P	LVDS	FPGA 0 SYSREF CLOCK
SYSREF#	71	FPGA0_SYSREF_N	LVDS	
SYSREF_REQ	57	PLL_SYSREF_REQ	CMOS 3,3	FPGA 0 SYSREF REQUEST

Table 24. PLL connection table

12.2 MCU, CPLD & FPGA

Complete pinout configuration and connection scheme of the digital devices are present in the table page of the TPM_ADU_1_6_PINOUT.xlxs , [RD2].

The iTPM1.6 register map is available in the document [RD11]

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